Probing charge state degeneracy in silicon isolated double quantum dot
Progress on Isolated Si Dot Systems Since QIST 2008

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Hitachi Cambridge Laboratory

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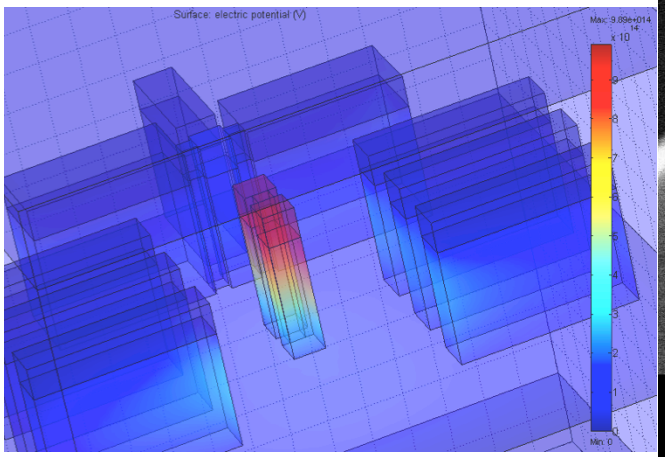
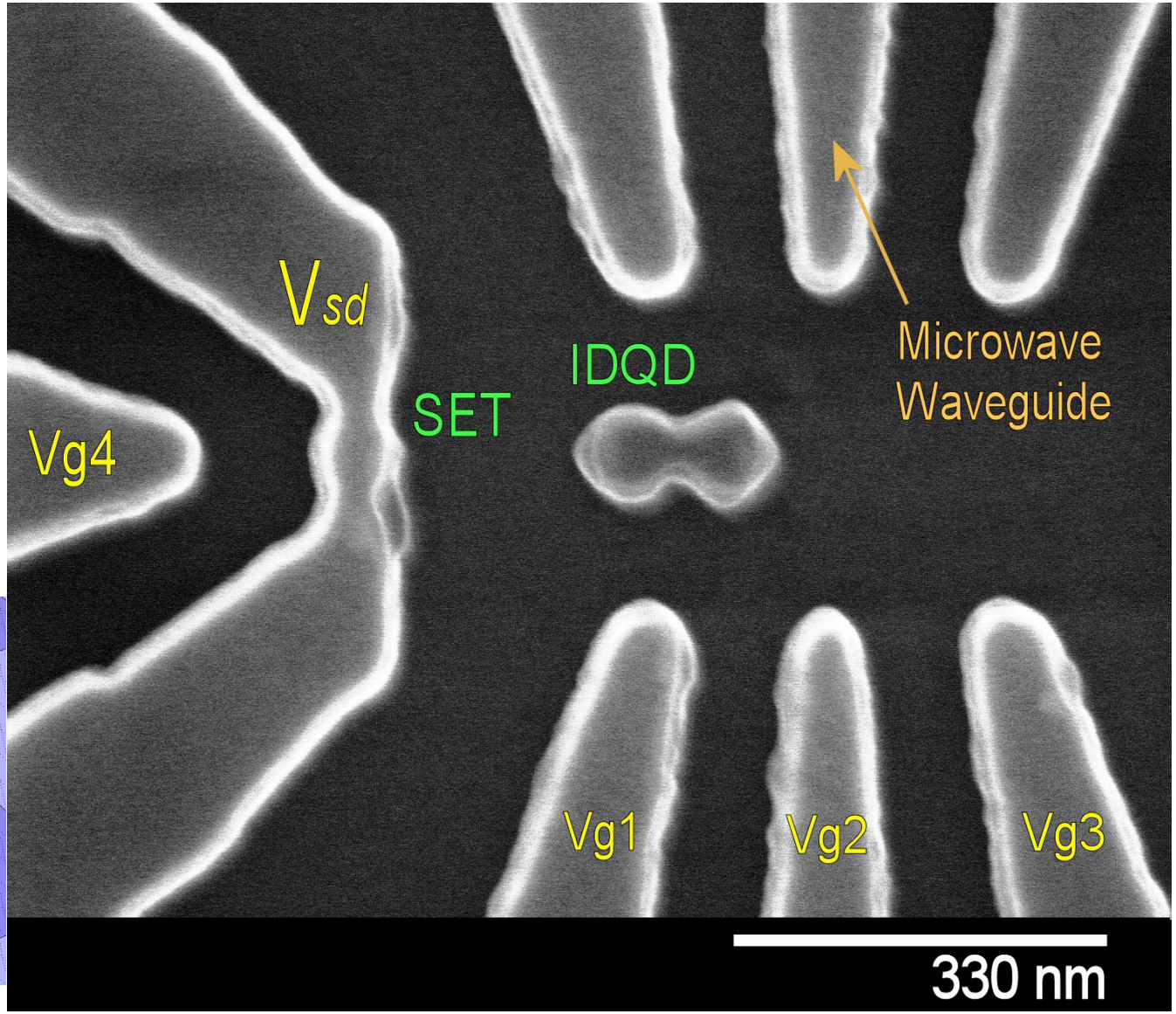
Qubit devices

- Methods of
- manipulation:
- DC
- High frequency:
  - Continuous wave
  - Pulsed





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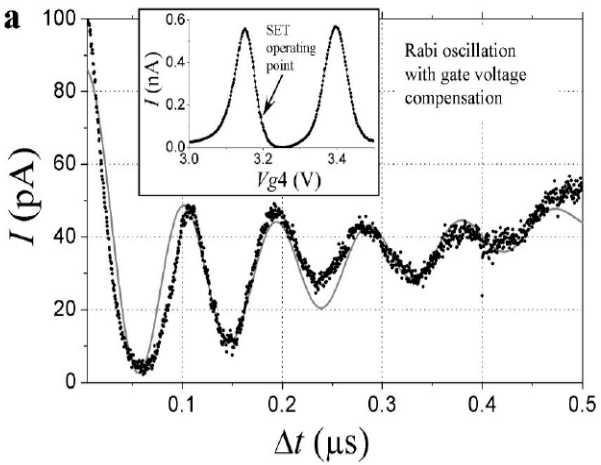
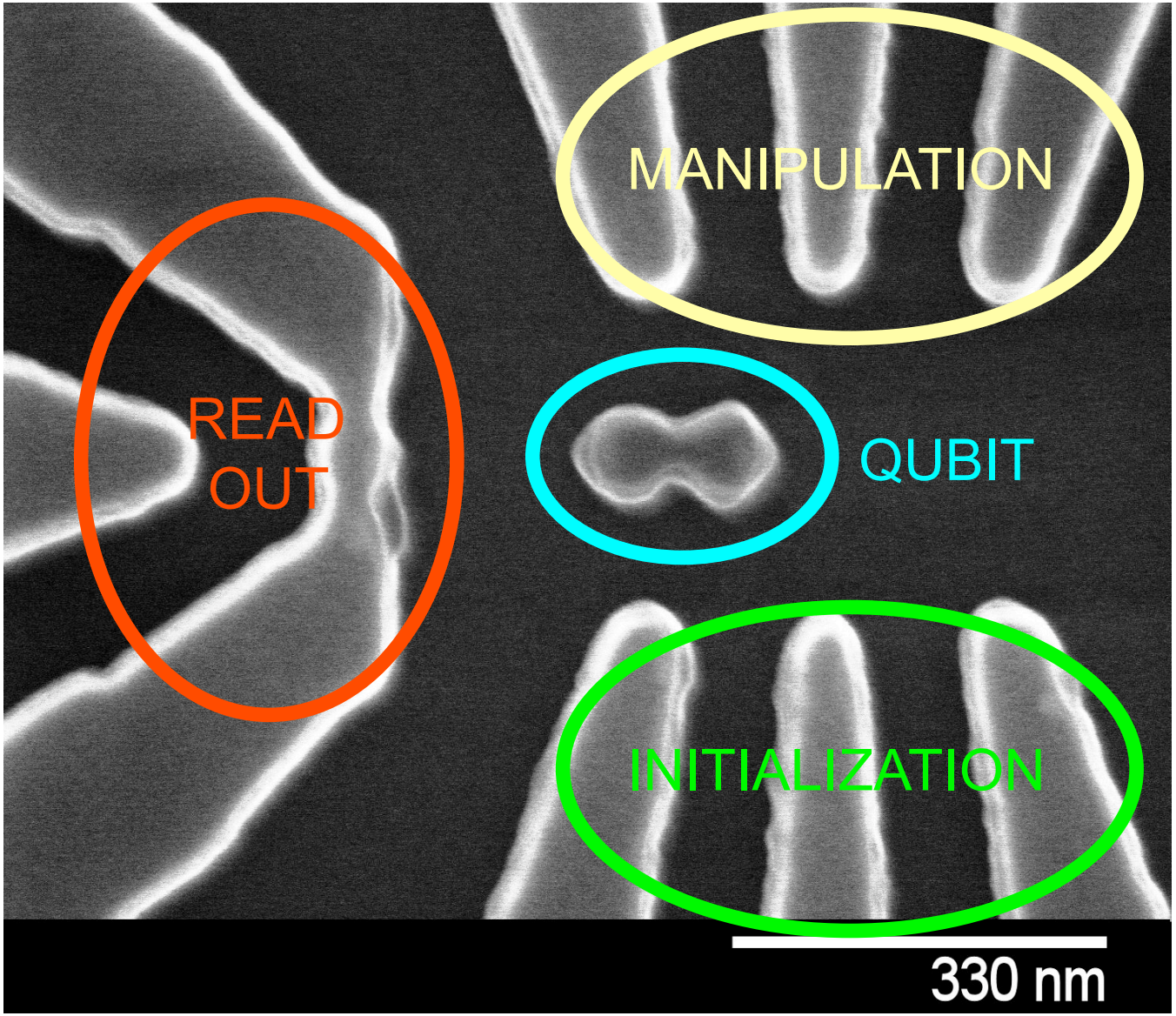




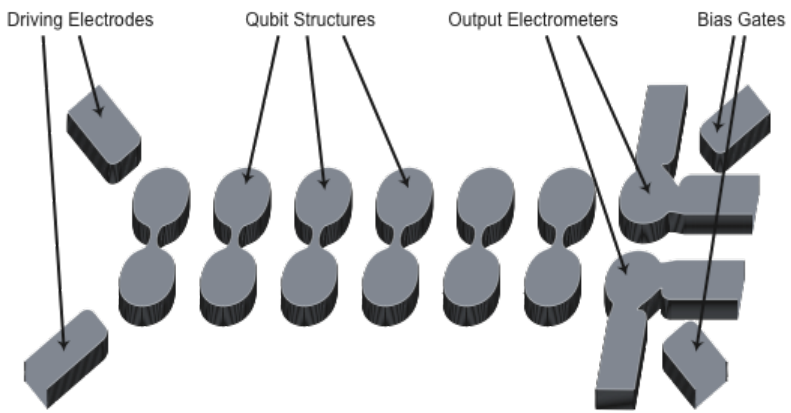
Silicon Charge Qubit

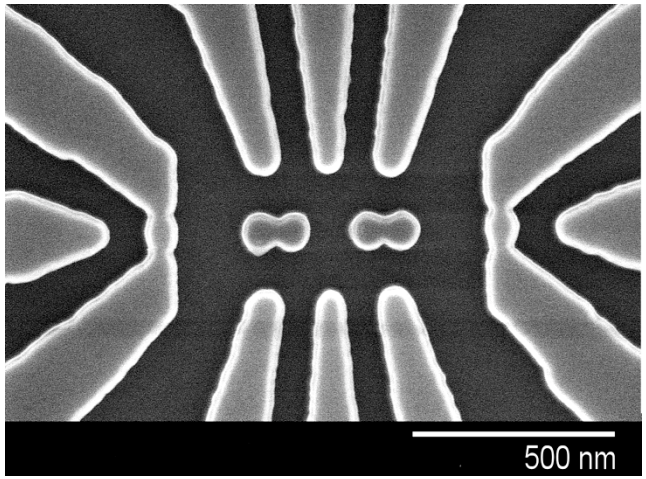
Long coherence time (200ns vs 2ns)

- Acoustic isolation
- Non-polar phonons

Standard processing techniques – reconvergence between physics experiments and production technology after several decades.

Easily scalable to 2-D arrays





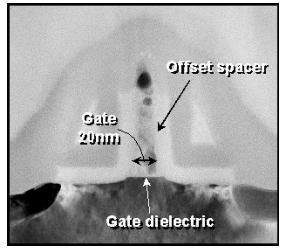
Are SOI Qubits a Realistic Technology?

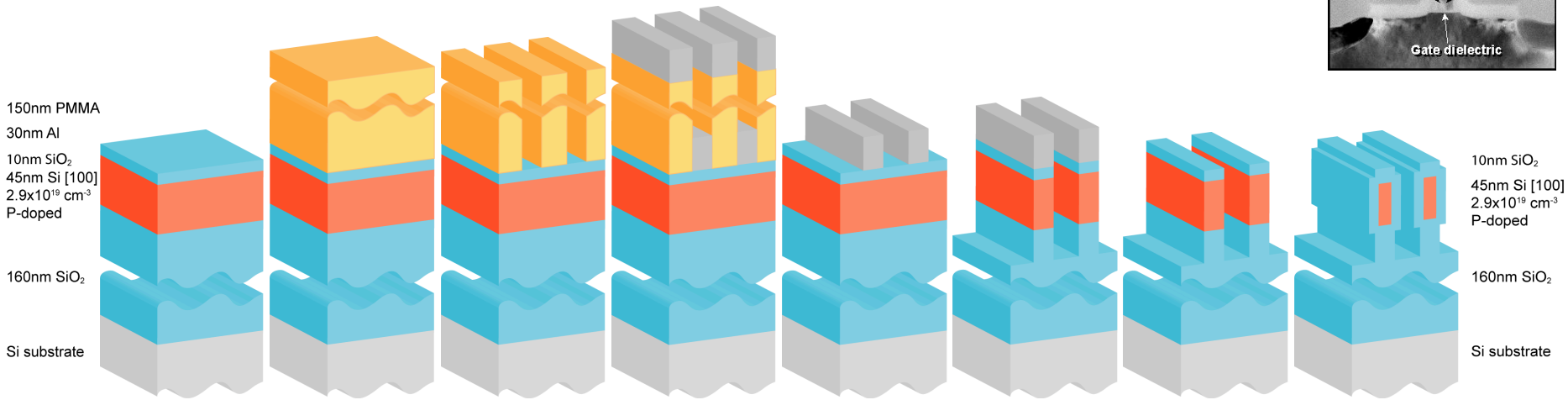
Open single and double quantum dot systems well understood for n and p type silicon-on-insulator and silicon:germanium-on-insulator

Isolated double quantum dot (IDQD) good for single qubit and promising for circuit scaling but difficult to analyse

Local fabrication – all processes except wafer growth within the same building - flexible, fast turnaround, but used for many materials - potential contamination?

Fabrication Process





Processing of highly doped silicon on insulator wafers through e-beam lithography of PMMA, followed by deposition of a sacrificial aluminium etch mask, reactive ion etching deep into the BOX layer, and oxidation to produce passivated trench isolated structures.

Questions

What is the dopant /trap type and distribution after fabrication?

How many electrons are on the dots after fabrication?

- Expect retention > 10 years
- Evidence for 10s rather than the 100s c.f dopant density

Which electron states are we using as the qubit?

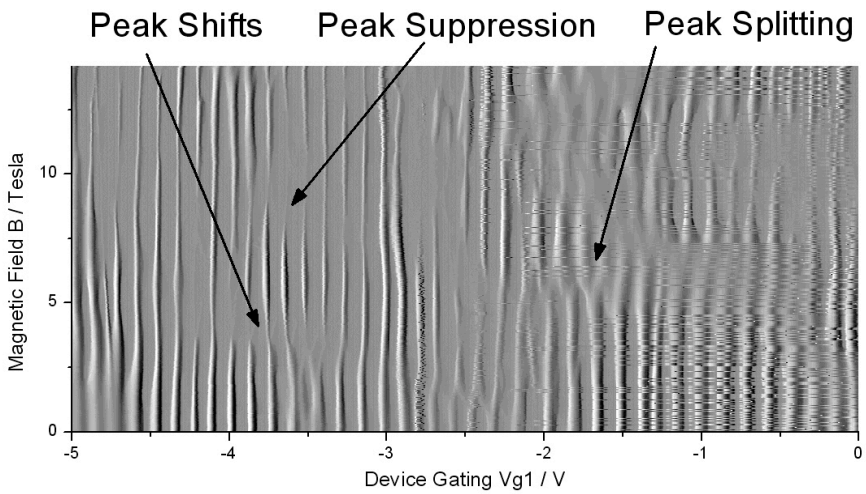
Reproducibility?

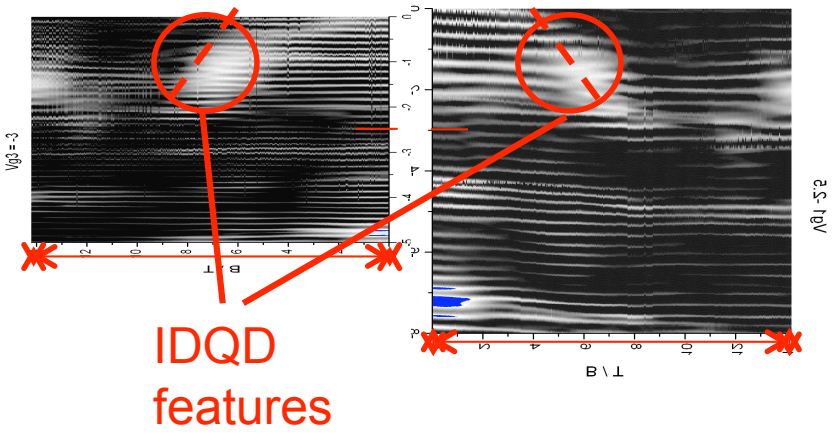
- Batch – batch variability usually >> device - device

Control experiments?

Questions

We see a complex response of the circuit in DC, pulse and microwave excitation and with magnetic field – which parts are due to the qubit?





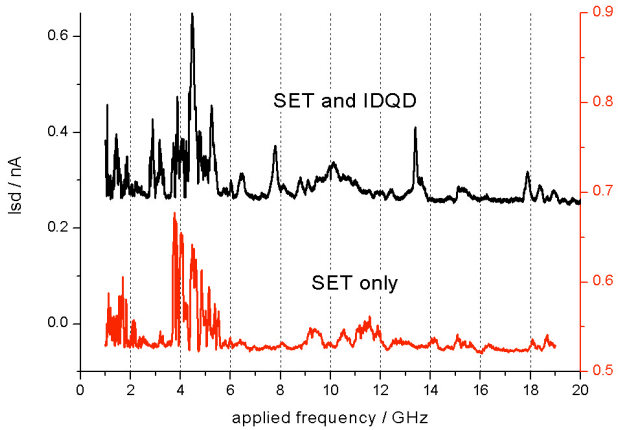
Peak shifts, splitting, and suppression are observed in contrast to SET only devices, suggesting control of spin related phenomena in the IDQD

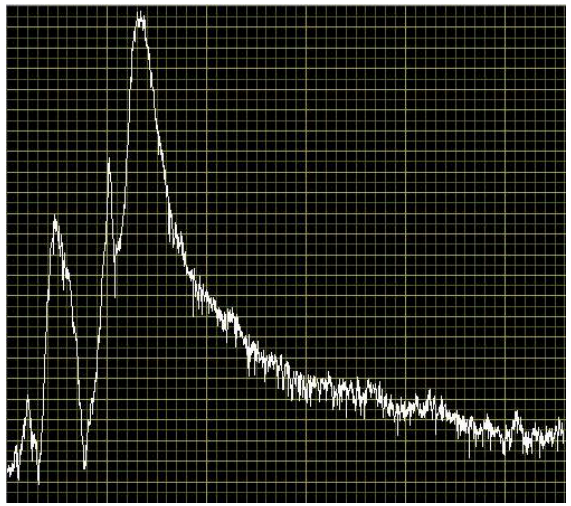
IDQD features matched up – from Vg3:Vg1 gate stability plot angles

IDQD features should line up, the SET CB should not

Questions

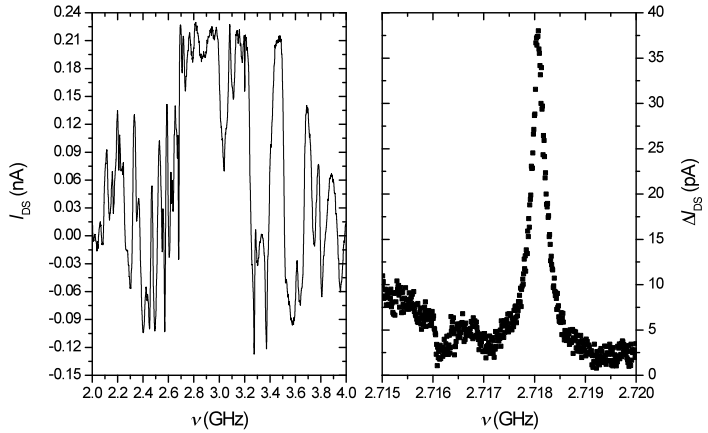
We see a complex response of the circuit in DC, pulse and microwave excitation and with magnetic field – which parts are due to the qubit?





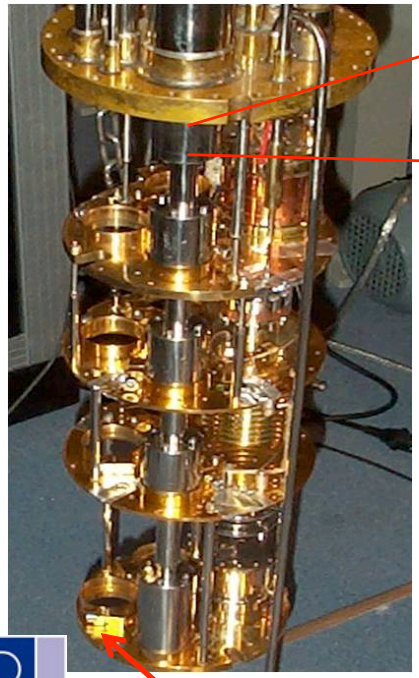
Microwaves successfully couple to the devices

Wide range response, comparison shows features in IDQD sweep that are not present for the SET only.

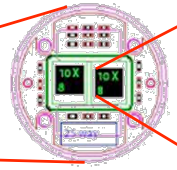


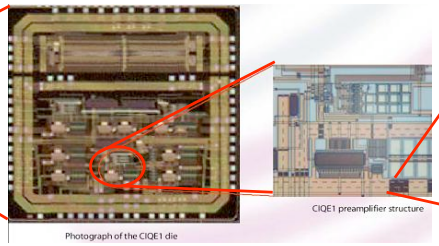
CIQE Measurement System

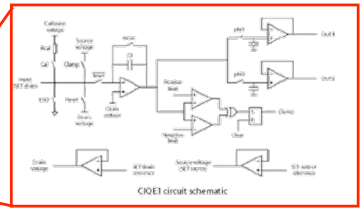
- Oxford Kelvinox 400

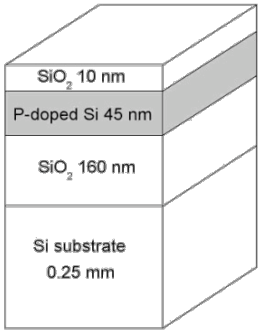


LT filters

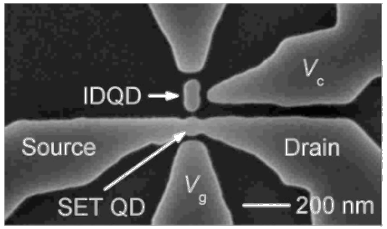




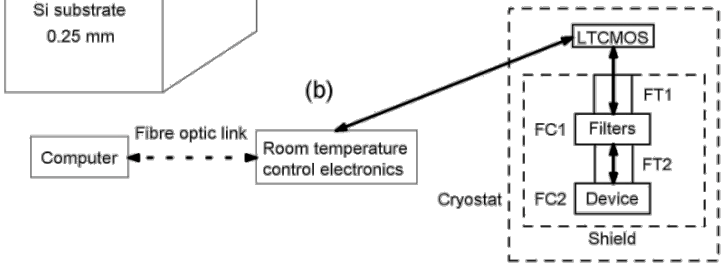




(a)



(b)



- LTCMOS at 4.2 K : voltages and measurement circuit, 100 kHz bandwidth
- Filters and faraday cages (FC) : noise suppression
  Feedthrough (FT) : EMI suppression > 10 MHz

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EPSRC Engineering and Physical Sciences Research Council

Device basic characteristics:

- Fine oscillations

  Periodic, reproducible

  May be shifted after thermal cycle

  Slope~0.25±0.01

- Background conductance

  Aperiodic, not reproducible over thermal cycle

  Linked to impurities

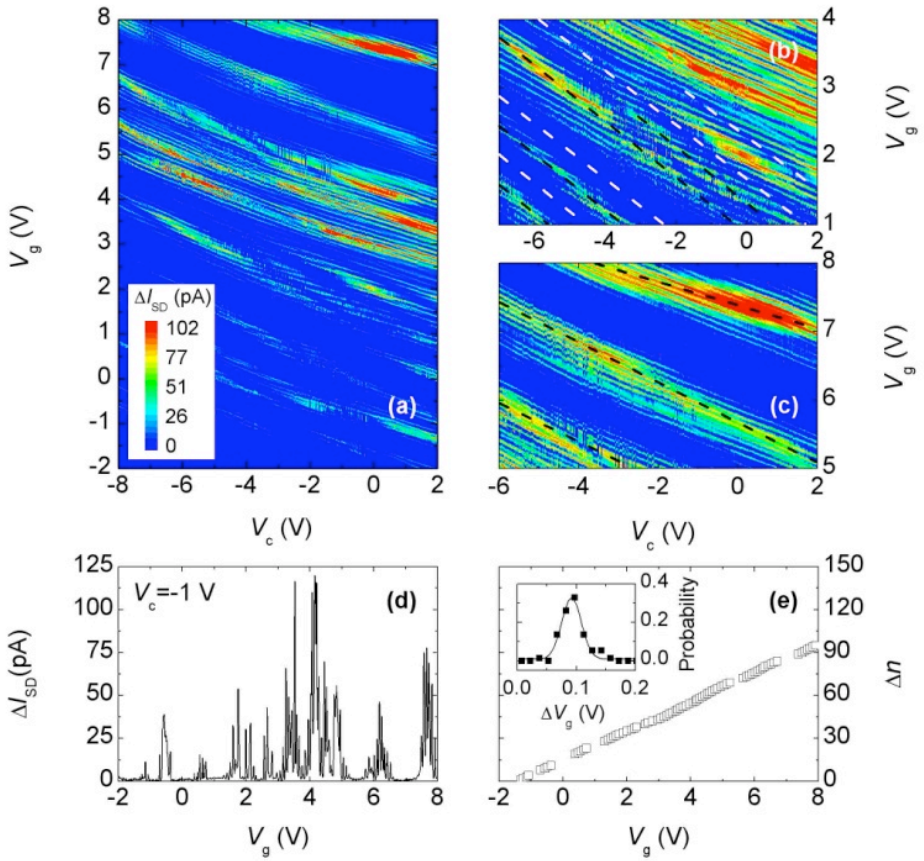
  Slope~0.23±0.06 (constant SET charge line)

- Secondary lines

  Near periodic, partly absent

  Linked to IDQD presence

  Slope~0.43±0.05 (IDQD charge motion change electrostatic potential)



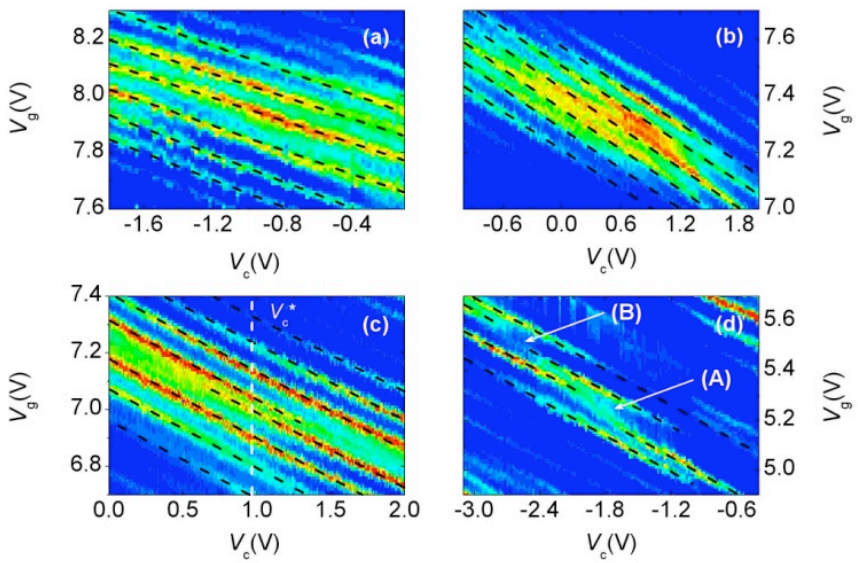
a) Gate dependency diagram
b) IDQD lines
c) Background conductance
d) Coulomb blockade oscillations
e) Periodicity and distribution

Coupling controlled by impurities?

- Different trap charges

Broken bonds between SiO_2 / ^4He, non-(100)
Sp2 between Si / SiO_2
Phosphorous in SiO_2 : $(POSi)^+$, PO_3^-…
Fast difuser : Na, Cu, Au, Cr…

Localised phosphorous :
MIT at ~ 3. 10^{18} cm^{-3} but disorder so
band tails up to N_d~ 4. 10^{19} cm^{-3} in 2D
effect enhanced in 0D



a) Normal Coulomb blockade conductivity peaks.
b) Disturbed peaks.
c) Shift of a single Coulomb peak
d) Shifts of Coulomb peaks with (A) and without (B) cotunneling.

- Consequences

Population of localised states controlled by gates
Electrostatic environment modified
SET-IDQD coupling is variable and mediated by impurities

Coulomb blockade shifts

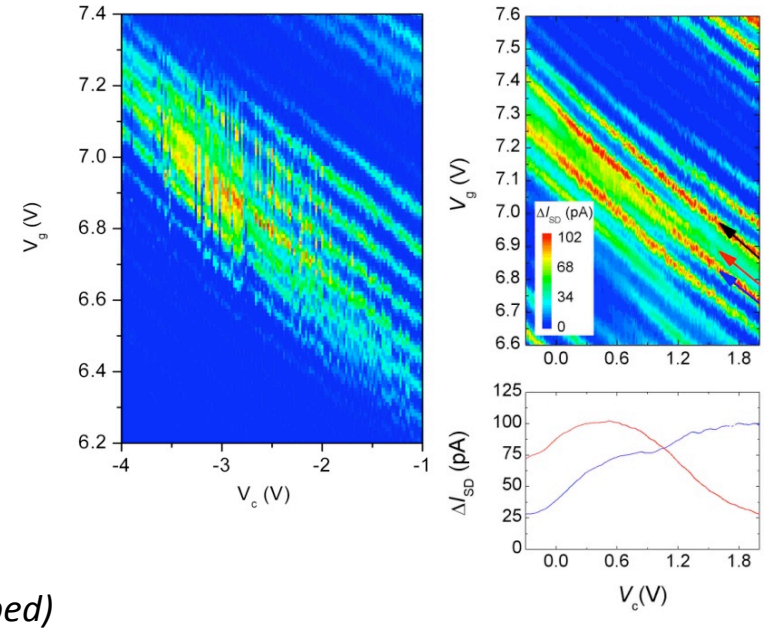
- Characteristics and origin

Reproducible within a same thermal cycle
At the crossing with IDQD lines

Not due to RTS (vertical lines)

Shifts~ $C_{SET\text{-}IDQD}/C_{\Sigma IDQD}$
About 50% of Coulomb period

From analysis for coupled SET-DQD
No more than 50% (neighbour CB lines undisturbed)
N → N+1 on each branches



RTS (left) and CB shift (right)

- Case : electron trapped close to SET island

Shift amplitude if classical capacitance calculation : Good
Slope, capacitance : Bad
$d_{SET\text{-}charge}$ ~ 20 nm so charge in etched region but no measure leakage : Bad

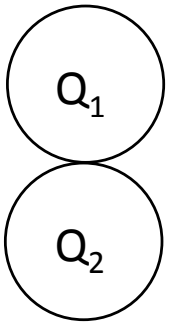
Charge motion detected by SET

- Charge motion in IDQD

Hexagonal structure for parallel dots

No charge transfer to SET, charge conserved

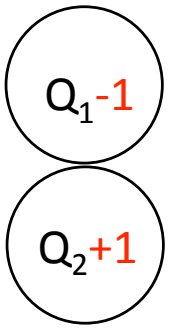
Charge re-organisation in IDQD



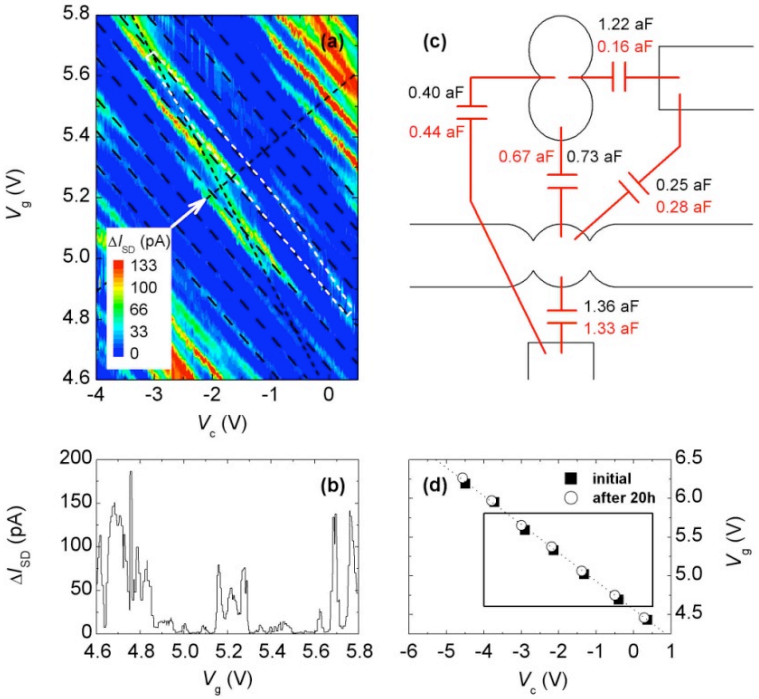
Low SET sensibility S1

High SET sensibility S2

$Q_{eff}=Q_1*S_1+Q_2*S_2$



$Q_{eff}=Q_1*S_1+Q_2*S_2+(S_2-S_1)$ → $\Delta Q=0$ but $\Delta Q_{eff}=S2-S1$



a) Hexagonal structure and its profile (b)
d) **Theoretical** and **experimental** capacitances
d) Structure stability

Tuning charge states in IDQD

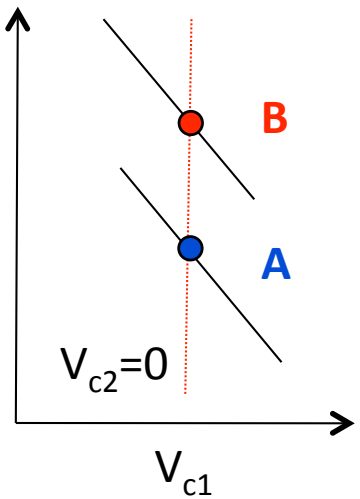
- V_{c2} used to tune IDQD population
- RTS events

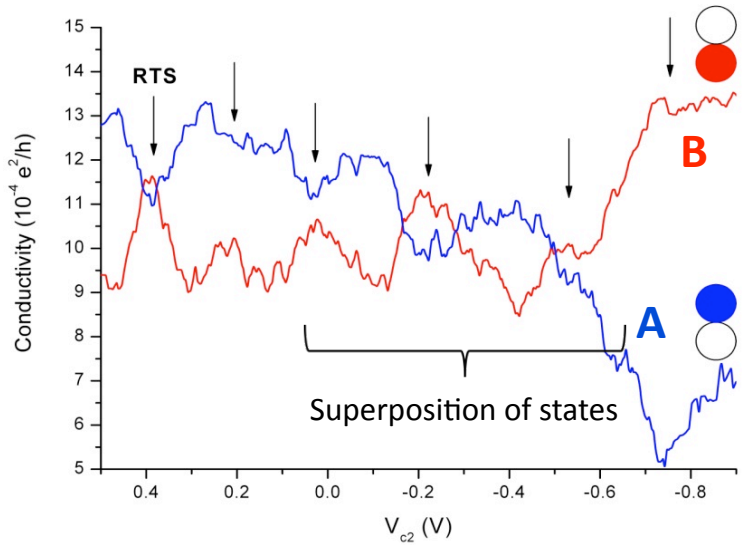
More present in degeneracy regions

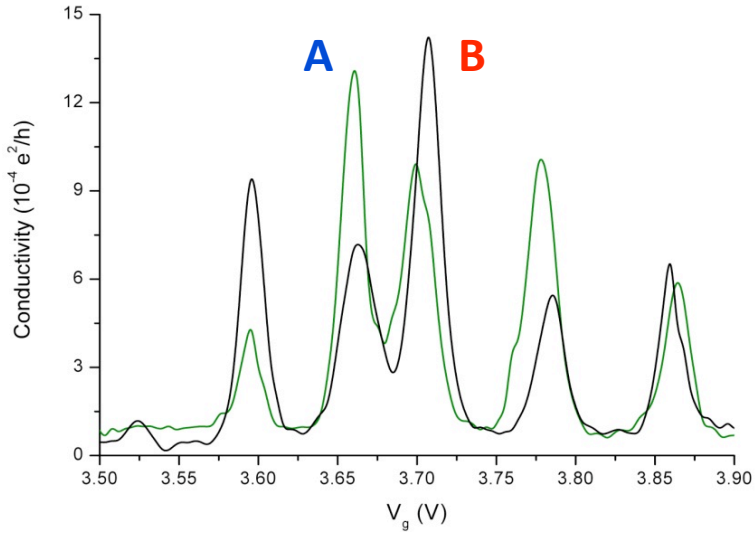
Shift **all** Coulomb peaks by the same amount

Induce population inversion on A and B

Not on other CB peaks

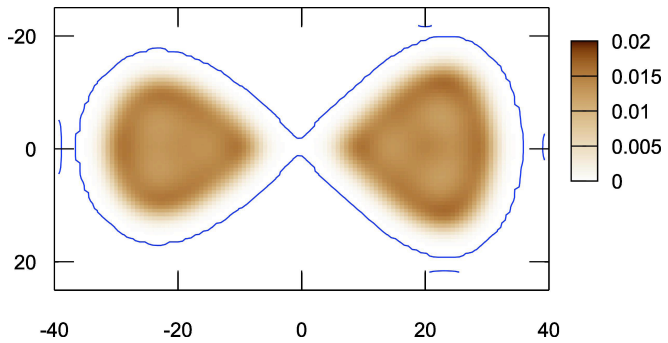




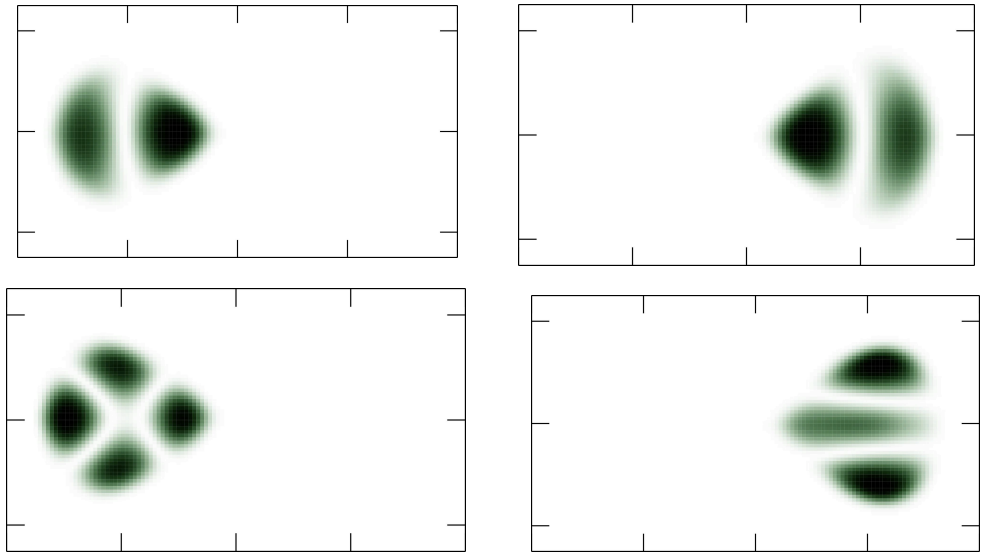


Which Electron States

charge density, 101 electrons



electronic wavefunctions d=2 nm

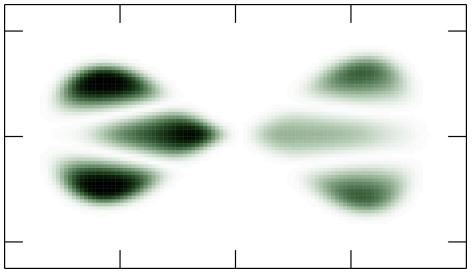


Finite difference method and anisotropic effective mass density functional theory (DFT)

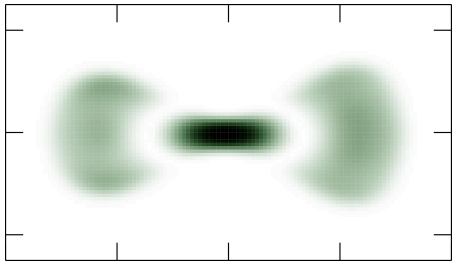
An optimised algorithm for determining the self-consistent DFT potential was used.

strong to weak coupling between 2nm and 5nm

D=5 nm



D=10 nm



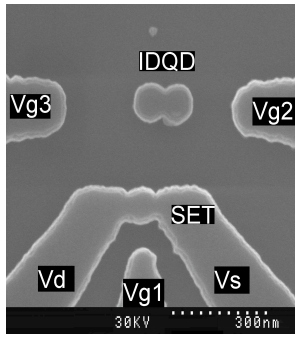
Aleksey Andreev, Phil Howard
Also at Surrey University

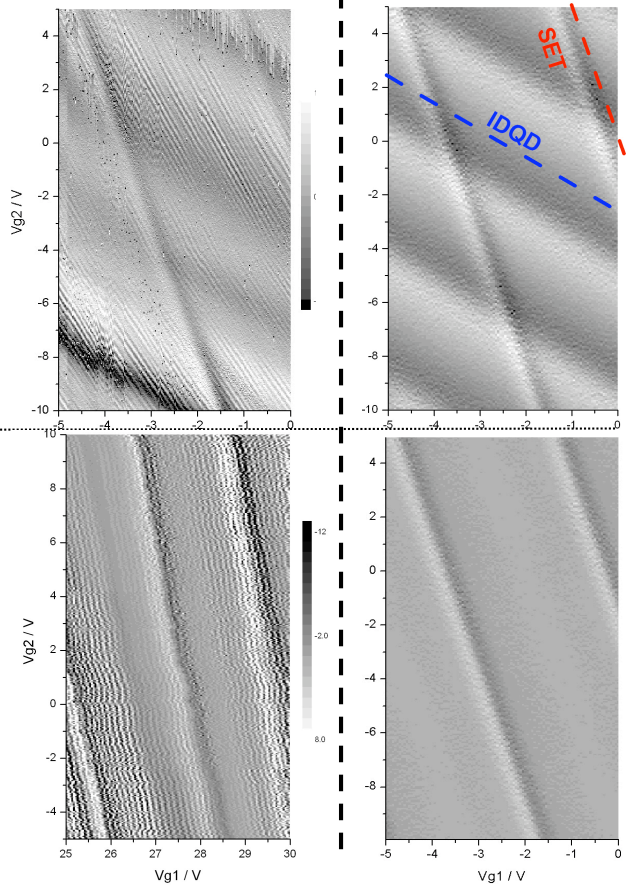
Control Experiments

Qubit charge state characterisation

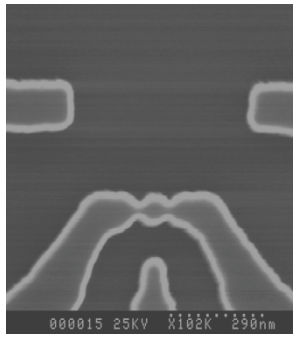
Experiment vs. Simulation

with IDQD





no IDQD

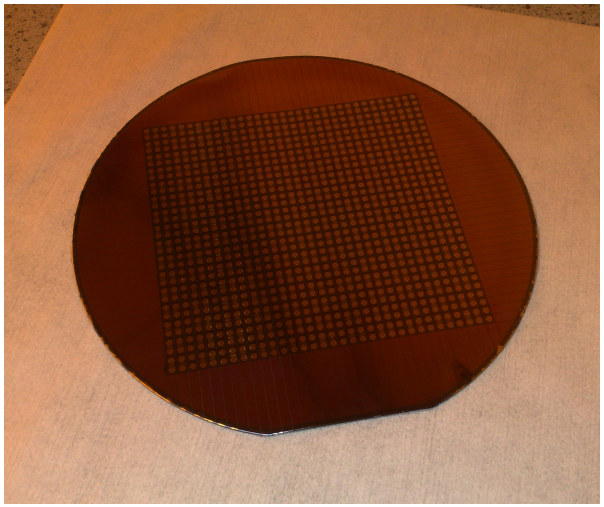


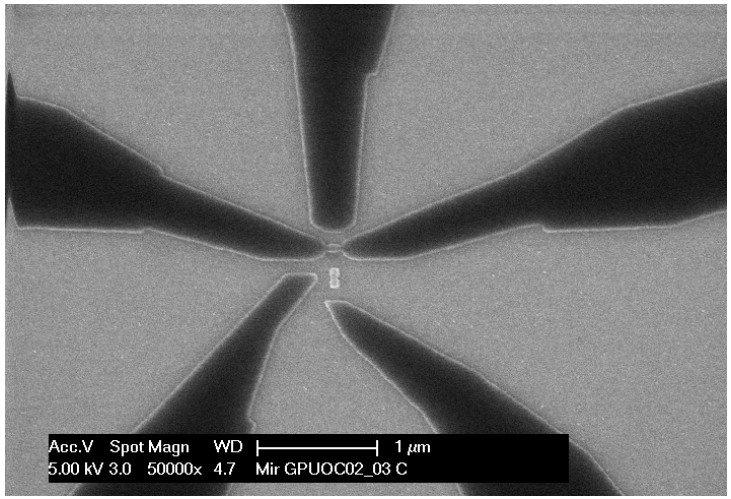
Simulation and experiment show well characterised charge polarisation of the IDQD (Qubit) structure, observed through the SET

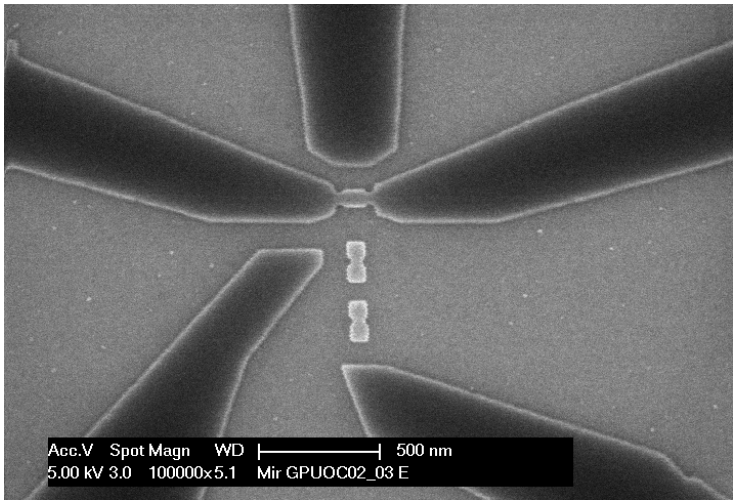
- Qubit charge state control
- Qubit charge state readout

Fabrication of new devices

- Devices fabricated in dedicated silicon fab line
- Nearly 4000 devices covering a variety of dimensions / device types
  - SETs
  - IDQDs in 'horizontal' and 'vertical' orientations
  - Multi-Qubit Devices
  - Connected double dots etc…

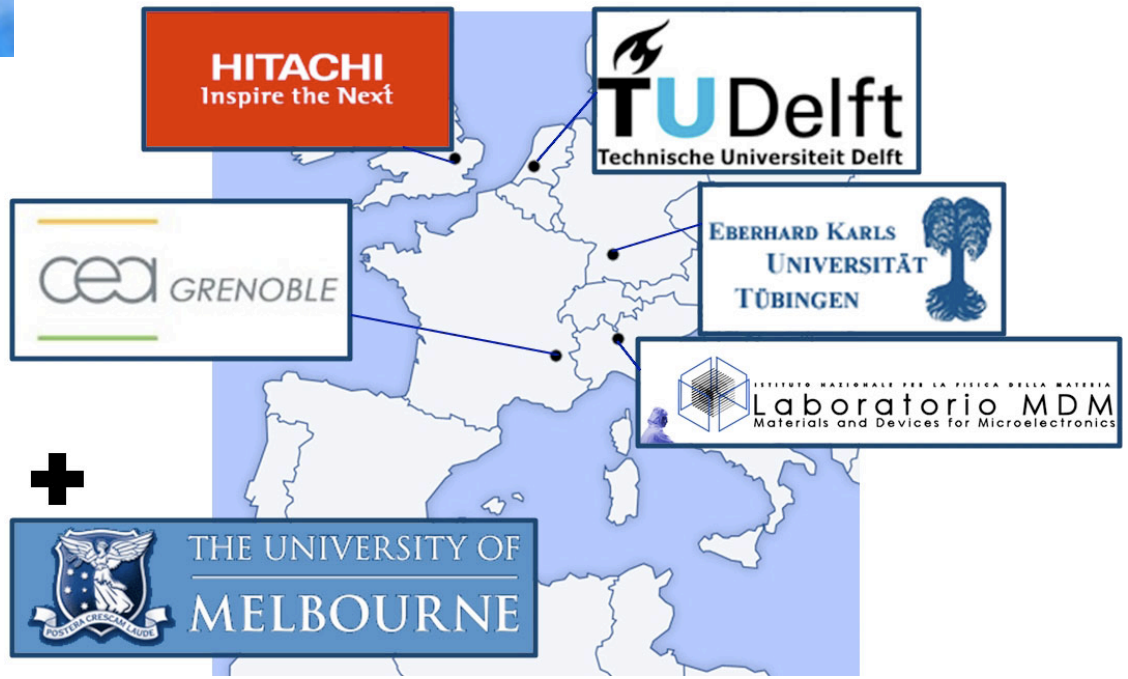




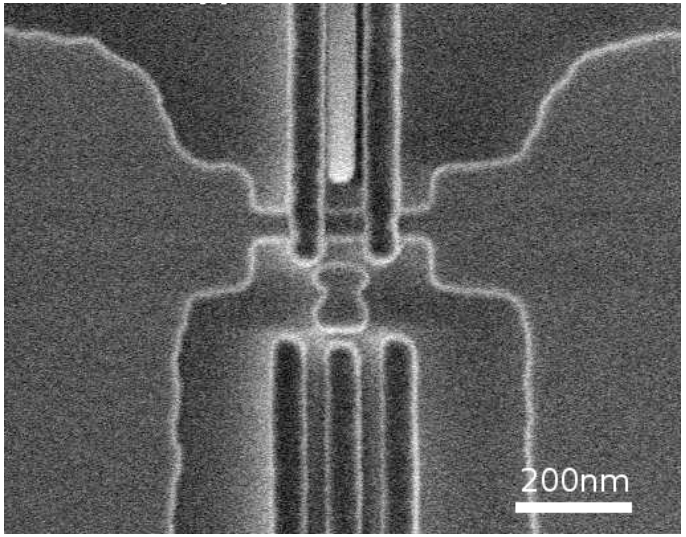


Atomic Functionality of Silicon Devices

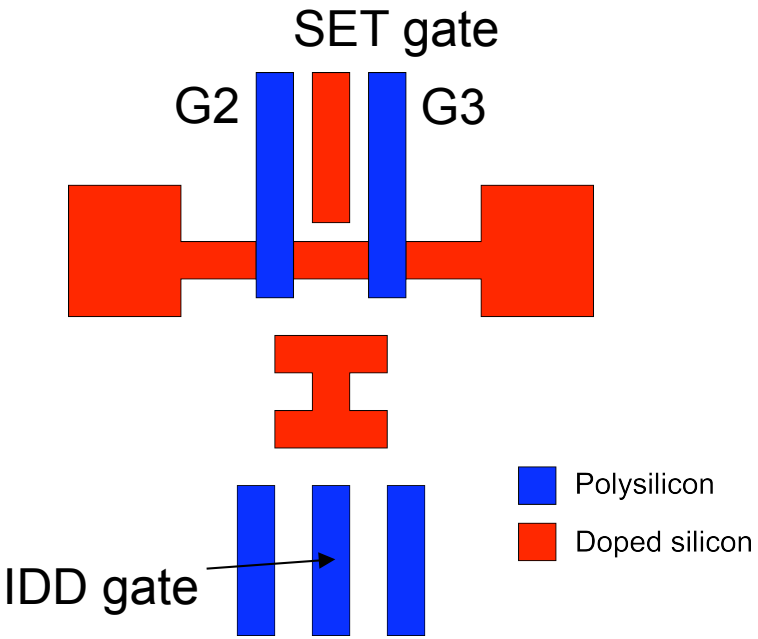
Marc Sanquer, Sven Rogge
Talks tomorrow



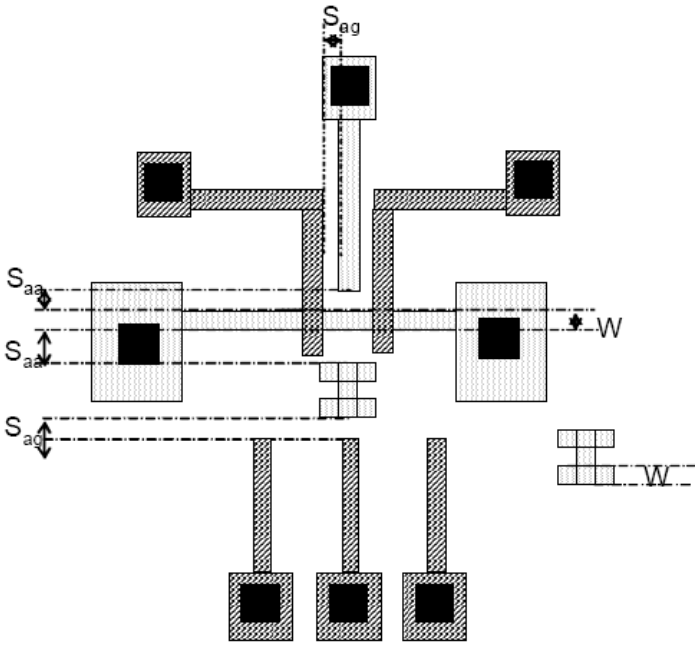
AFSID devices



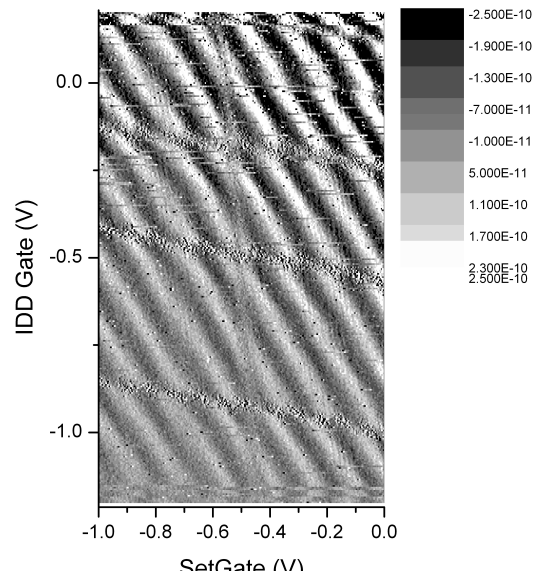
- AFSID EU project
- Isolated Double Quantum Dot devices
  - Line width 40nm
  - Doped to 10^{19} Cm^{-3} with As
  - Polysilicon shields area underneath during implantation

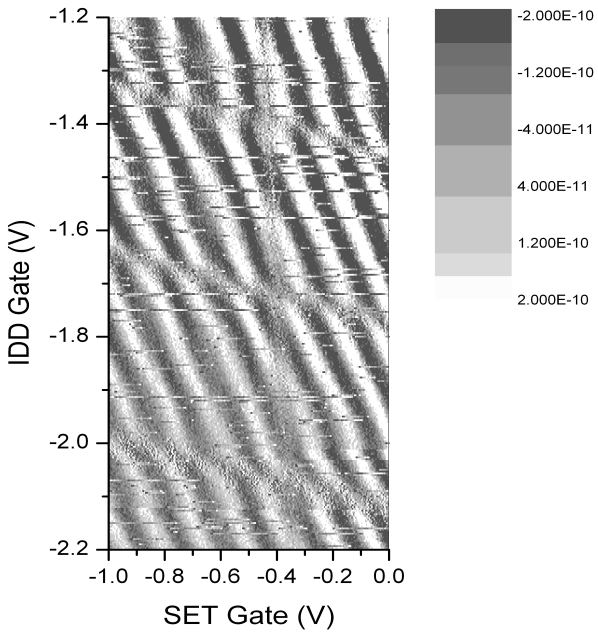


Geometry and electrostatics different



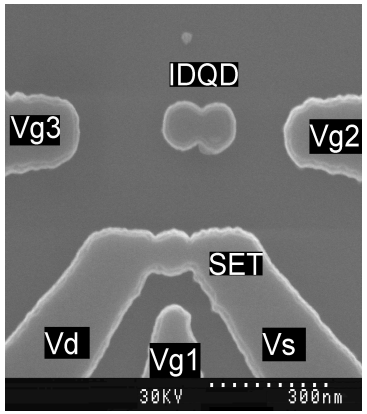
AFSID devices – IDD polarisation

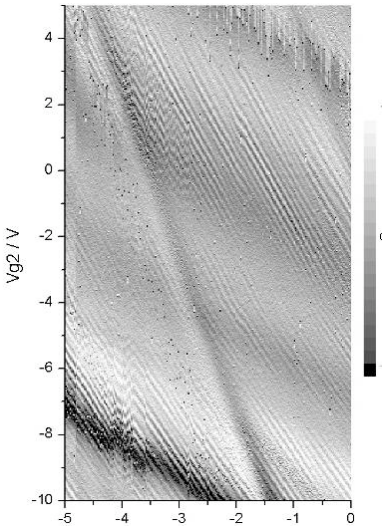


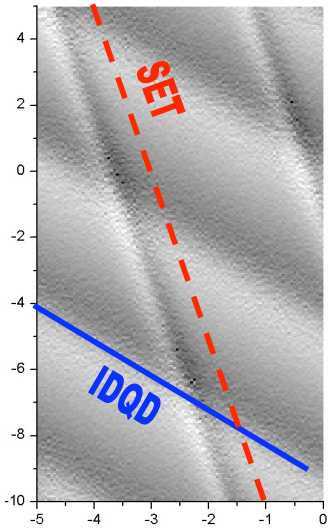


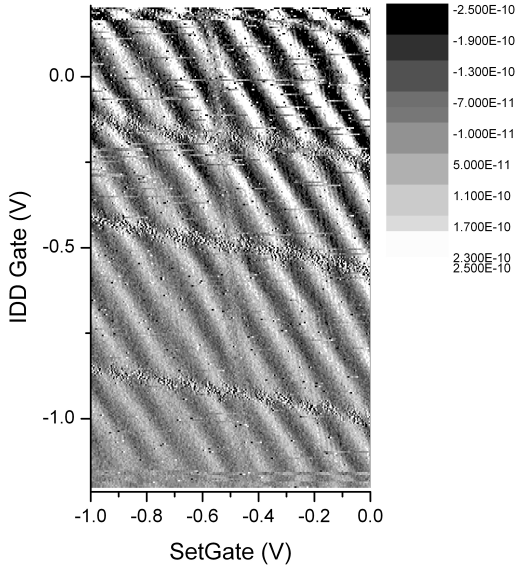
- Measuring SET gate VS IDD gate at 4.2K
- 3 sets of features
  - CB oscillations
  - Near vertical shift
    - strongly coupled to SET gate
    - trap near SET?
  - Repeated near horizontal bands causing shifts in the CB oscillations
    - strongly coupled to IDD gate
    - Multiple bands as far as IDD gate was taken
    - Charge redistribution in IDD

AFSID devices - measurement





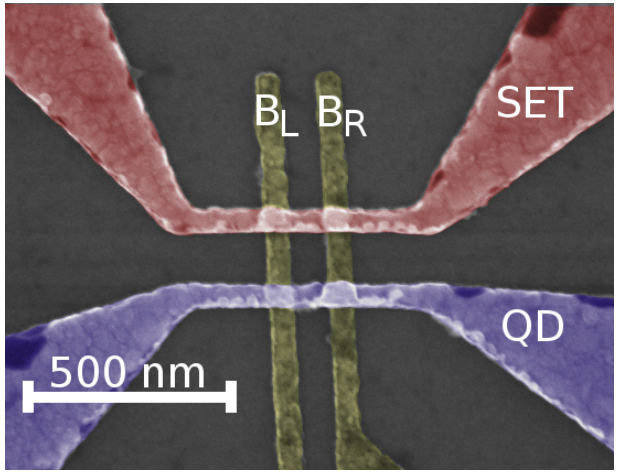


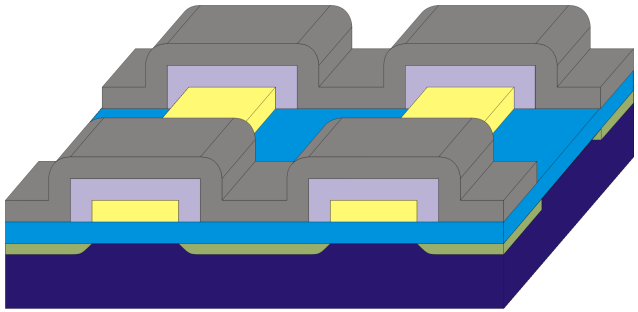


Experiment Simulation AFSID

- Comparison of trench isolated SET / IDQD device with AFSID device
  - IDQD features much more closely spaced in AFSID
  - Peak shifts more clearly visible in AFSID device due to stronger coupling of IDD to SET
  - AFSID devices show sharp transitions promising for microwave manipulation of IDD states
  - Non-uniform distribution of IDD polarisation lines meaning individual transitions can be addressed by microwaves

Surface gated silicon device





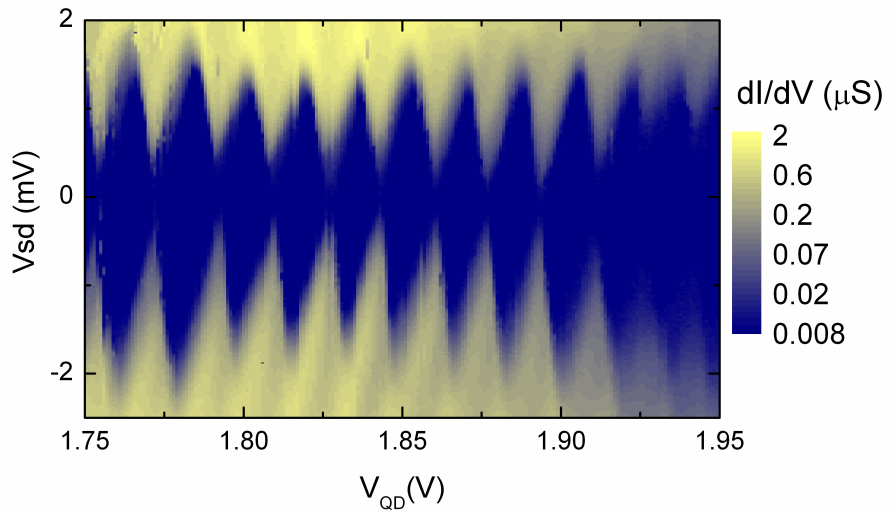
- Intrinsic Silicon Substrate
- Si02
- Aluminium Oxide
- Aluminium (gate)
- Aluminium (barrier)
- 2DEG

- Device electrostatically formed in intrinsic silicon
  - Two layers of aluminium gates
    - Top gates induce 2DEG
    - Lower gates locally deplete to form tunnel barriers
    - Electrically isolated by aluminium oxide
  - Common barrier gates for ease of fabrication and increased device yield
- Consists of QD and neighbouring SET to detect charges
  - Dot dimensions 50 x 85 nm
  - Device separation 125 nm

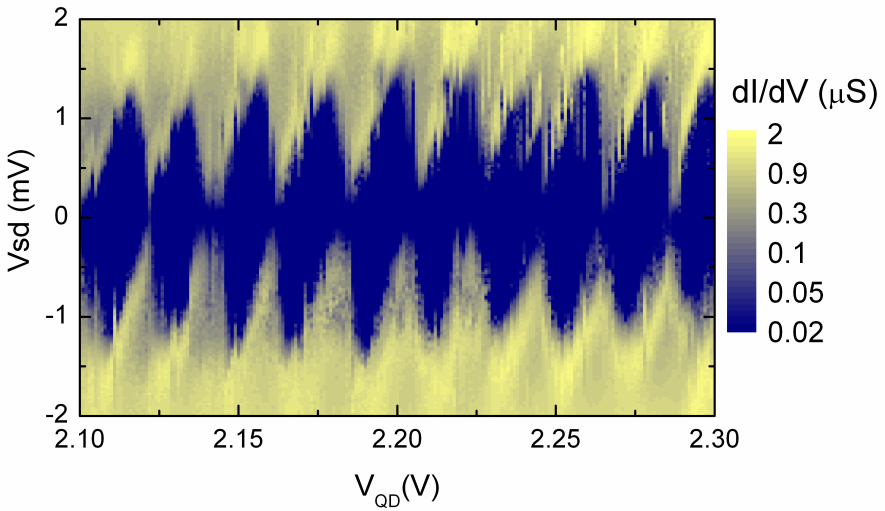
Gareth Podd, Susan Angus, Andrew Ferguson
Poster this evening

Surface gated silicon device - characterisation

QD

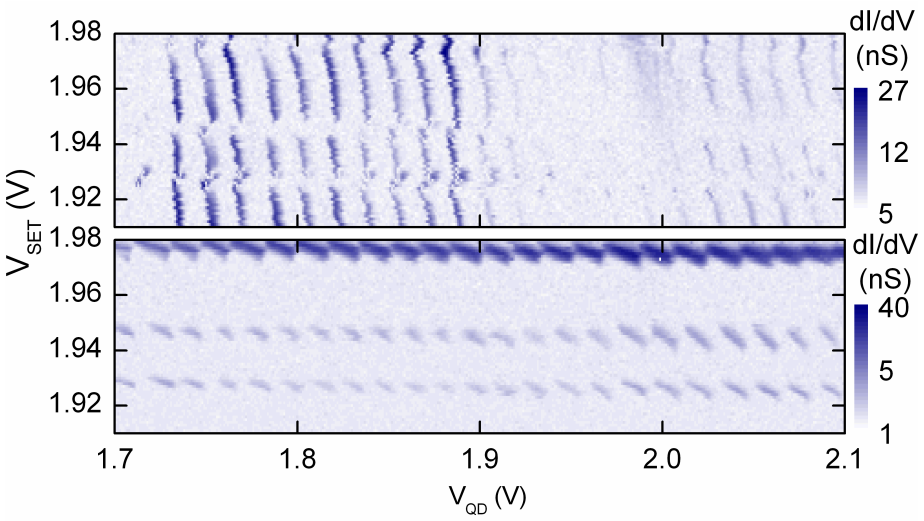


SET

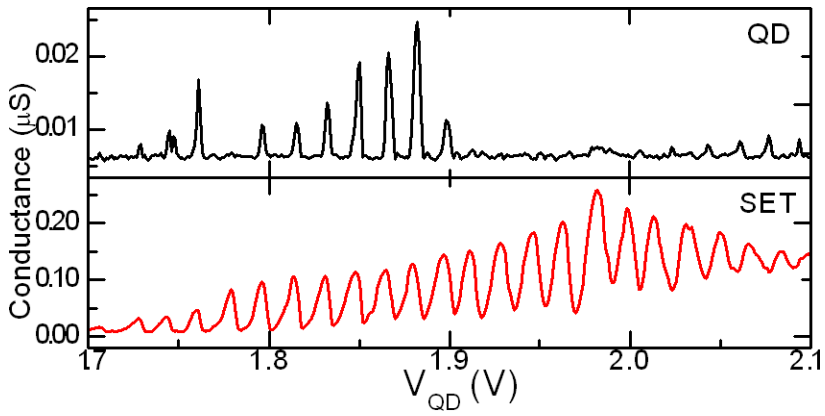


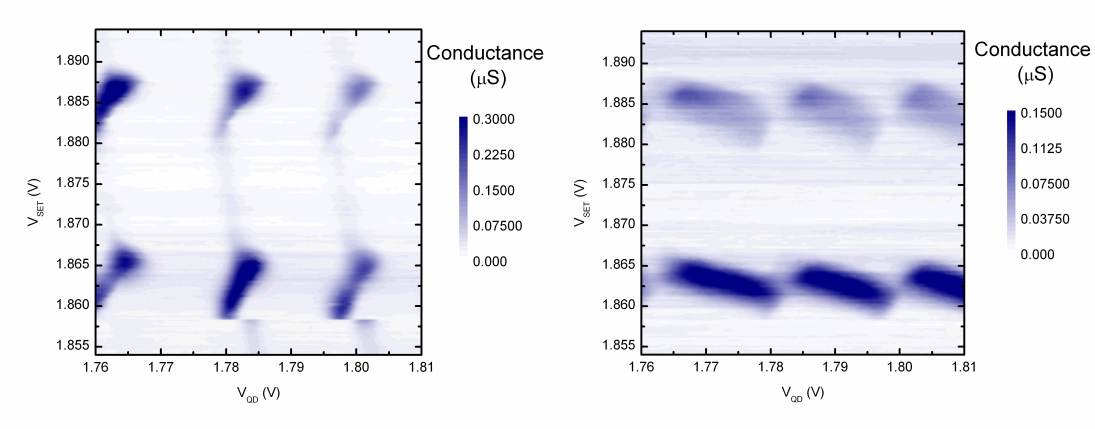
- Barriers tuned to operating point where multiple oscillations observed in both devices
  - More in QD than SET
  - Difficult to optimise due to constraints of common barriers
- Devices characterised individually – with no 2DEG induced in opposite device
  - Device parameters in good agreement with simple parallel plate capacitance model

Surface gated silicon device – charge sensing



- Simultaneous measurement of both devices
  - Vertical QD oscillations, horizontal SET
  - Charge detection ~ 0.2 e
  - Clearly observed even when transport current through QD small





Are SOI Qubits a Realistic Technology?

Structures which have the same circuit and device topology, yet are fabricated by very different means, show consistent similarities and differences

~50nm SOI devices fabricated in-house
~50nm SOI devices fabricated by regular fabline
<40nm SOI devices with shallow etch geometry
Surface gated silicon devices

Still considerable work needed for a full characterisation

Probing charge state degeneracy in silicon isolated double quantum dot
Progress on Isolated Si Dot Systems Since QIST 2008

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