Cryogenic CMOS electronics for single charge readout

Sandia Electronics Team

Kevin Eng, Tom Gurrieri, Erin Longoria, Ralph Young, Jason Hamlett, James Levy, Malcolm Carroll

University of Maryland

Akin Arturk, Siddharth Potbhare, Marty Peckerar.

Funding support:

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

Silicon Qubit Workshop '09

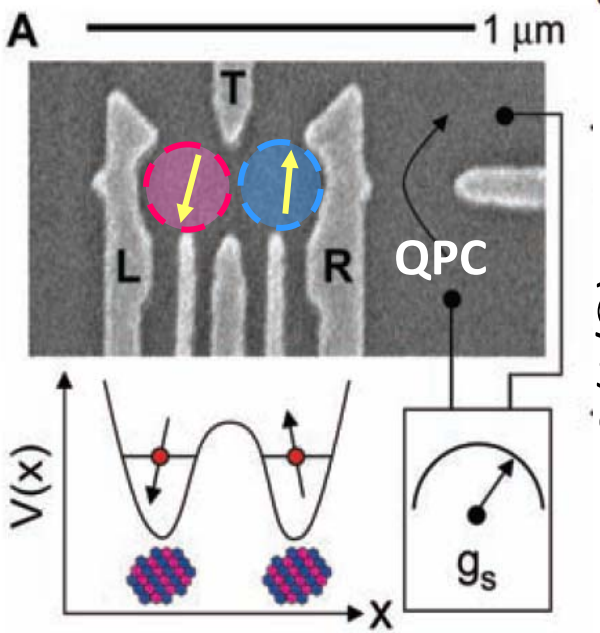
Solid State Qubit

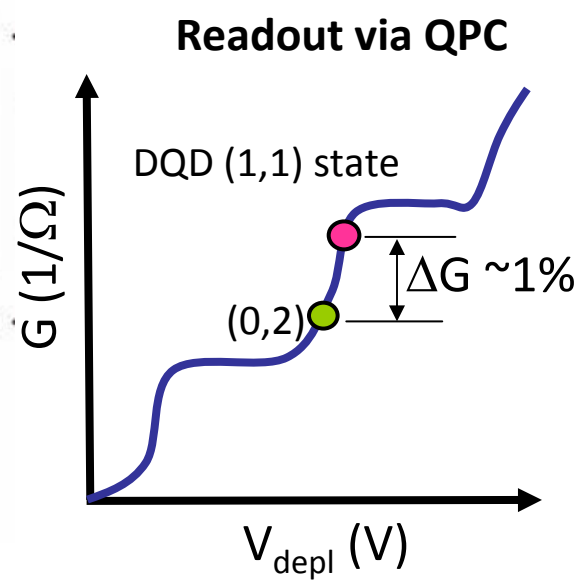
Science 2005

Coherent Manipulation of Coupled Electron Spins in Semiconductor Quantum Dots

J. R. Petta,[1] A. C. Johnson,[1] J. M. Taylor,[1] E. A. Laird,[1] A. Yacoby,[2] M. D. Lukin,[1] C. M. Marcus,[1] M. P. Hanson,[3] A. C. Gossard[3]

We demonstrated coherent control of a quantum two-level system based on two-electron spin states in a double quantum dot, allowing state preparation, ojective readout. These techniques are based on

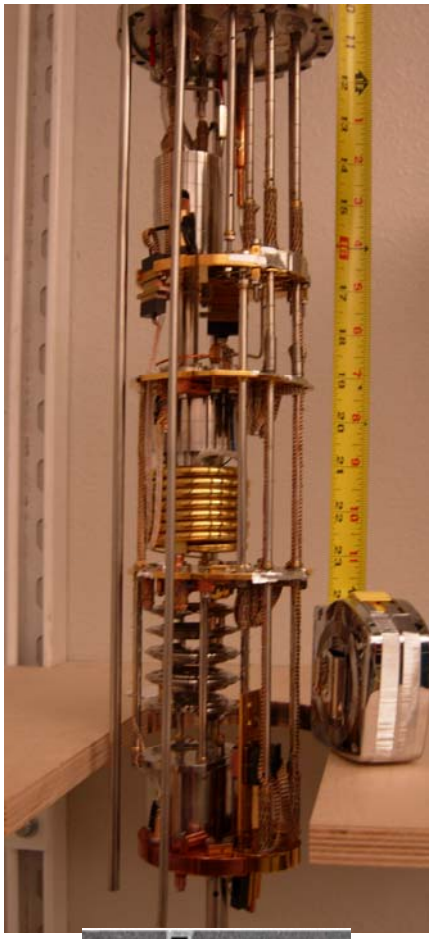


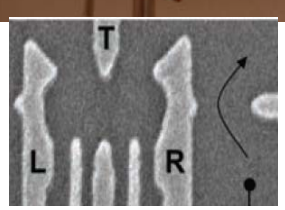


QPC charge detection:
M. Field *et al.*, (1993).

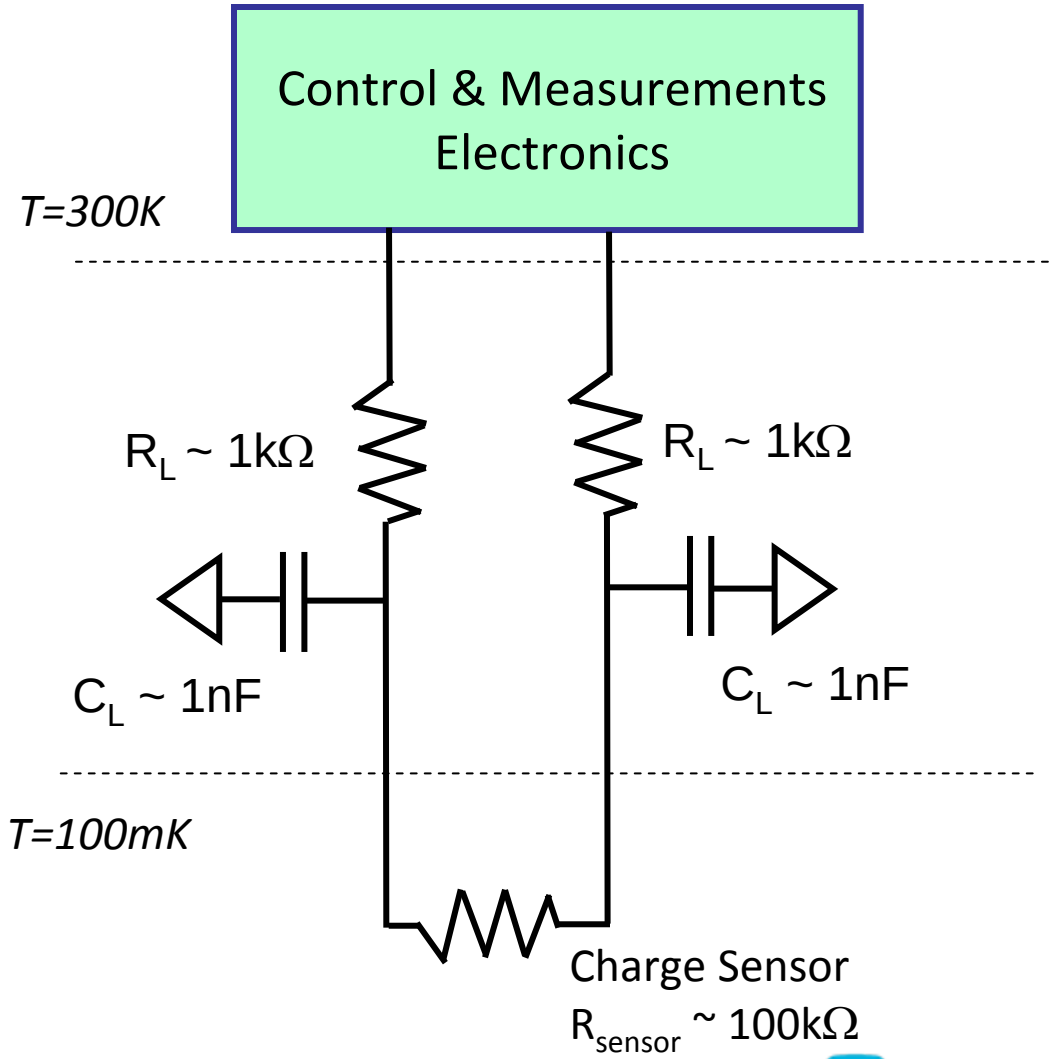
Challenge: Measure fast

Oxford MX400





Typical setup of measuring solid-state qubits



RF measurements on DQDs

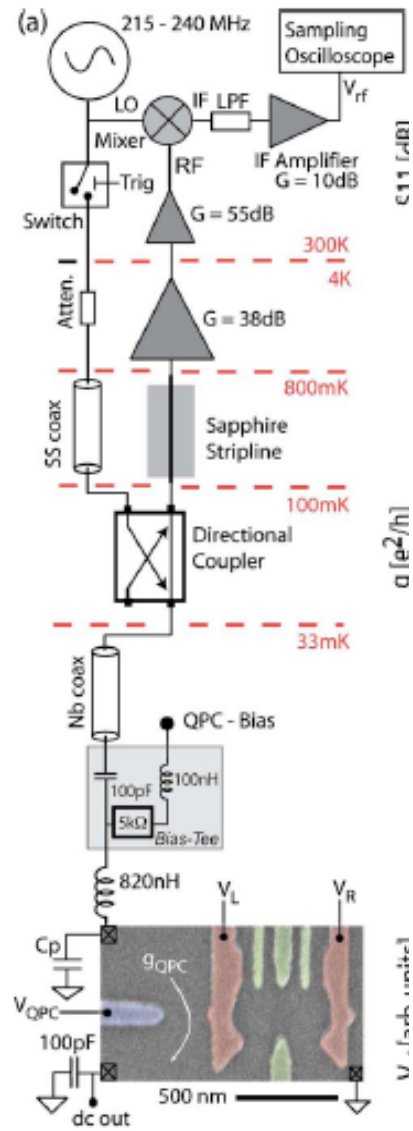
APPLIED PHYSICS LETTERS **91**, 162101 (2007)

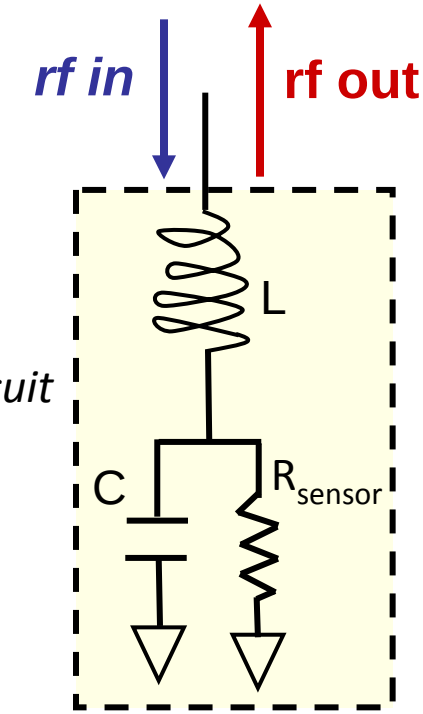
Fast single-charge sensing with a rf quantum point contact

D. J. Reilly and C. M. Marcus[a)]
Department of Physics, Harvard University, Cambridge, Massachusetts 02138, USA

M. P. Hanson and A. C. Gossard
Department of Materials, University of California, Santa Barbara, California 93106, USA

(Received 21 July 2007; accepted 28 August 2007; published online 15 October 2007)





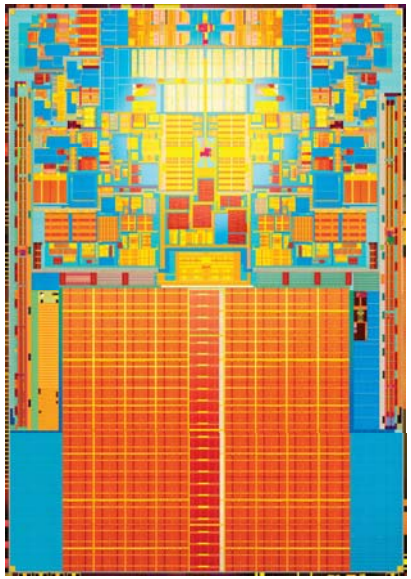
Overcome RC limitations by transforming R_{sensor} to 50Ω impedance

R. J. Schoelkopf, et al., Science (1998)

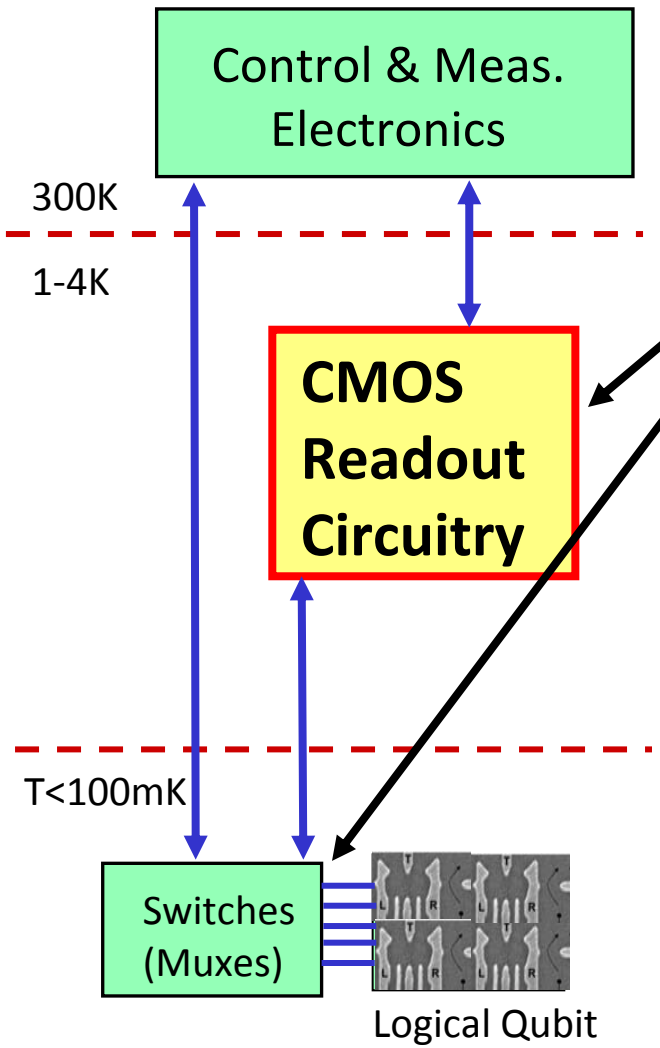
Tank circuit
Z = 50Ω

See Poster by L. Tracy

Can CMOS provide fast & sensitive measurements?



CMOS Digital Readout

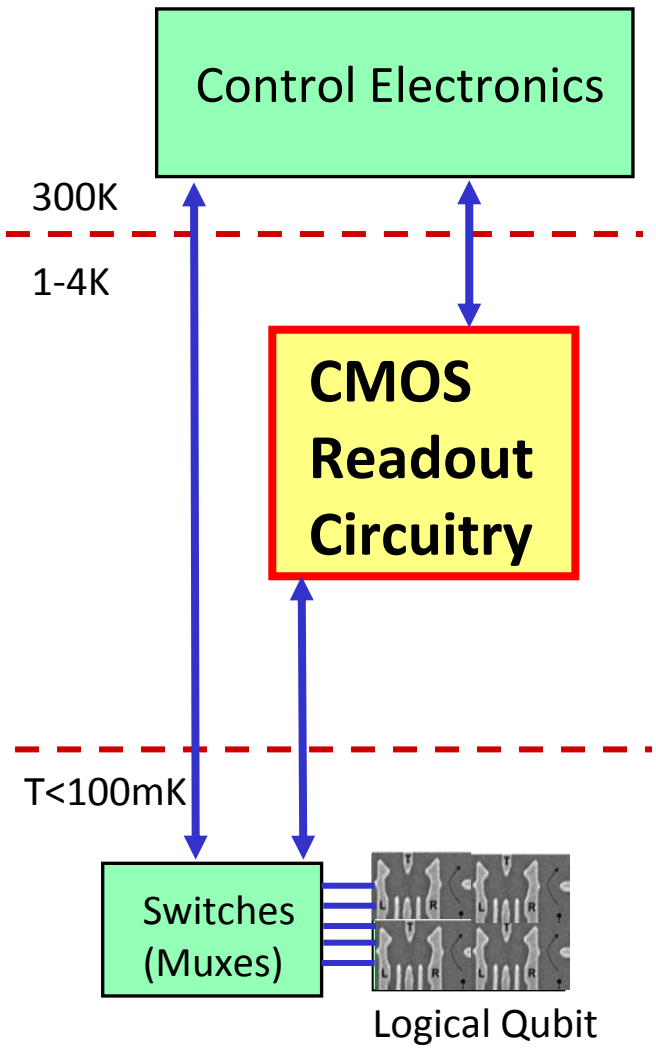


Long Term:

Can cryo-CMOS circuits support readout of multiple qubits?

See Poster by J.E. Levy

CMOS Digital Readout



	Digital Read-out	RF Reflectometry
Read-out Type	Digital	Continuous
Area	Monolithic	Discretes
Stand Alone Measurement Speed	~ nsec.	~ µsec.
Matching of multi read-out	Excellent	Poor (relies on parasitics)
Muxing of multi read-out	Easy	Difficult

*** Is it possible to achieve CMOS potential?**

Outline

Sandia's Cryo-CMOS effort:

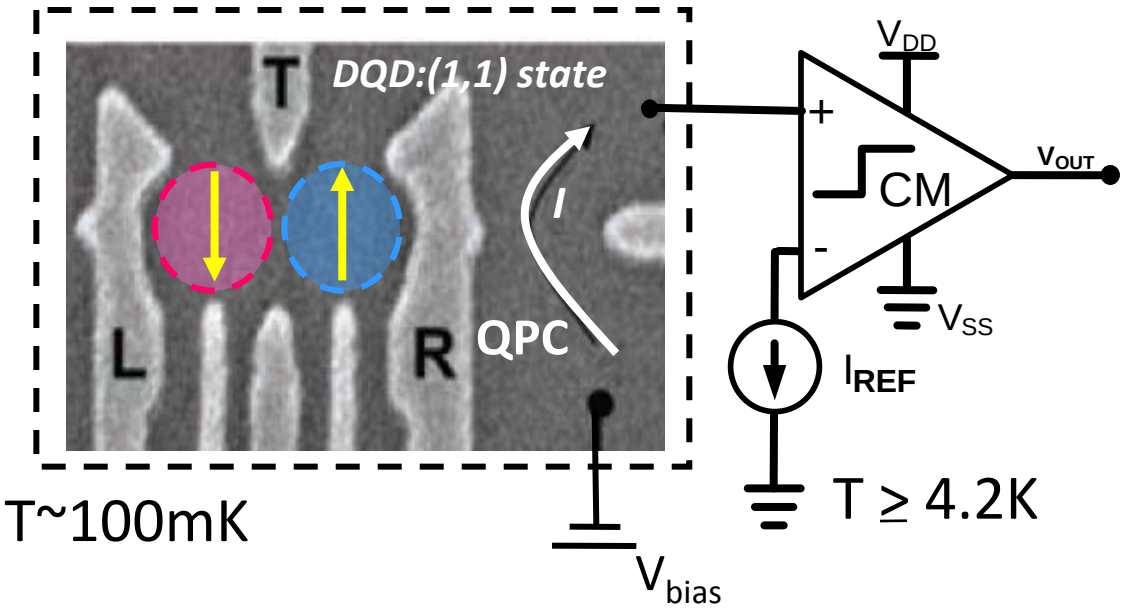
- Digital readout scheme
- Sandia's foundry process
- Performance of 1st generation CMOS circuits.

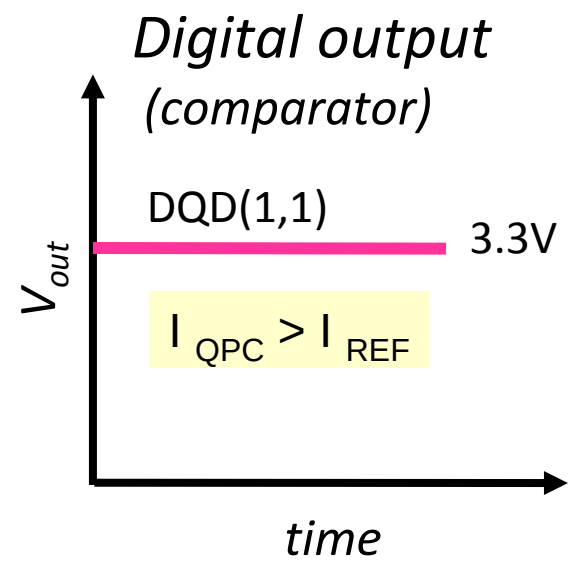
Work in Progress/Future:

- How can we improve/optimize circuits?
- Implementation?

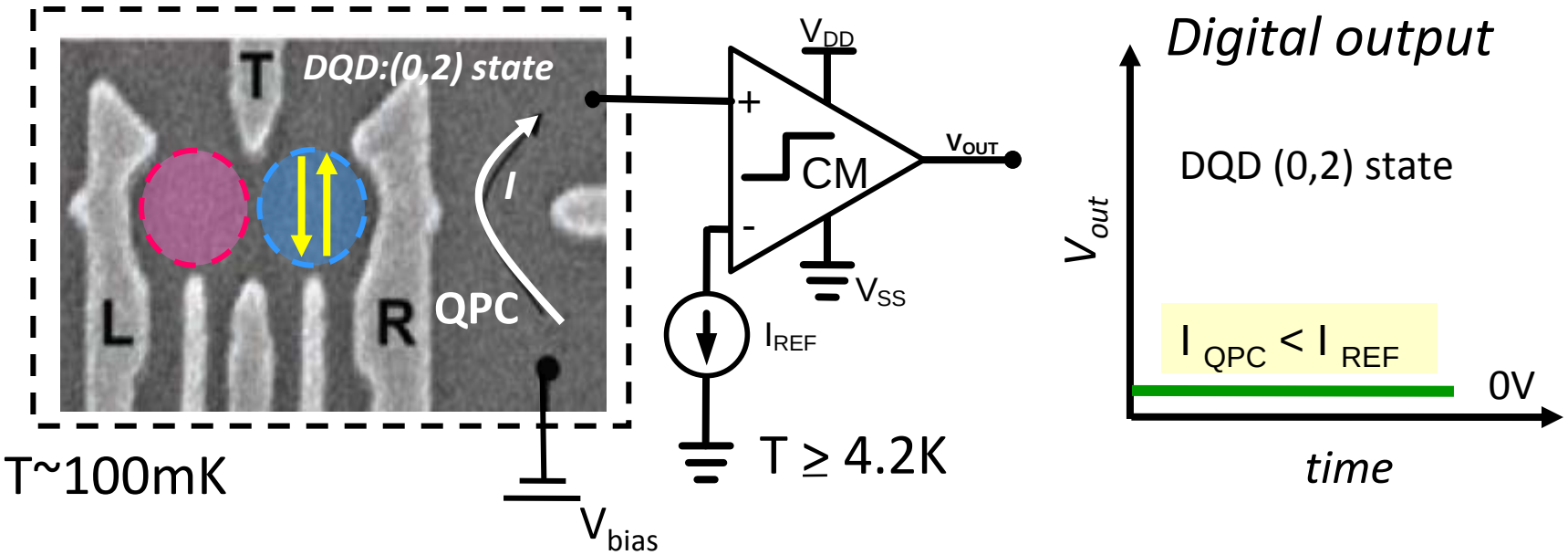
Readout: Current Comparator

Compares the changes of current in the QPC between the two states of the qubit

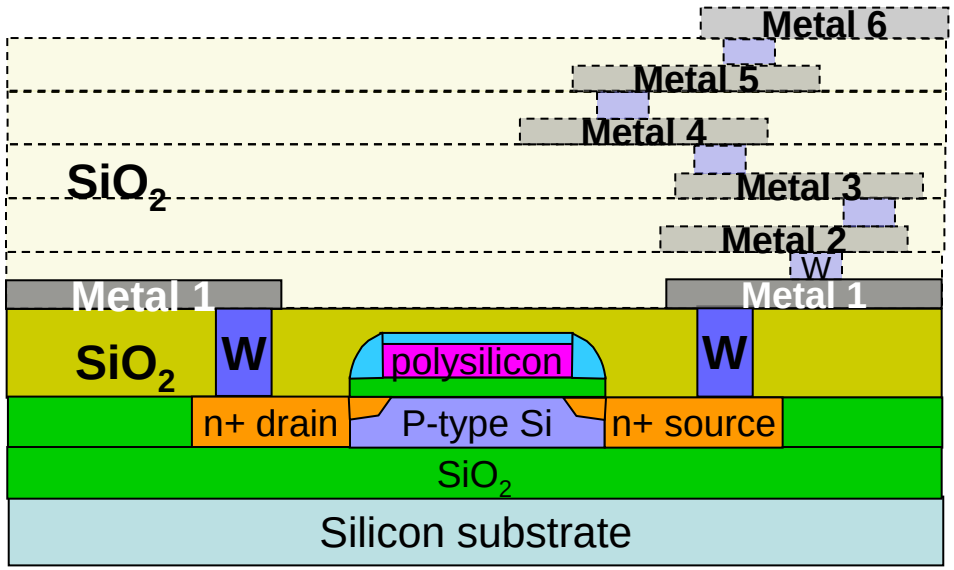




Readout: Current Comparator



Sandia's CMOS7 process

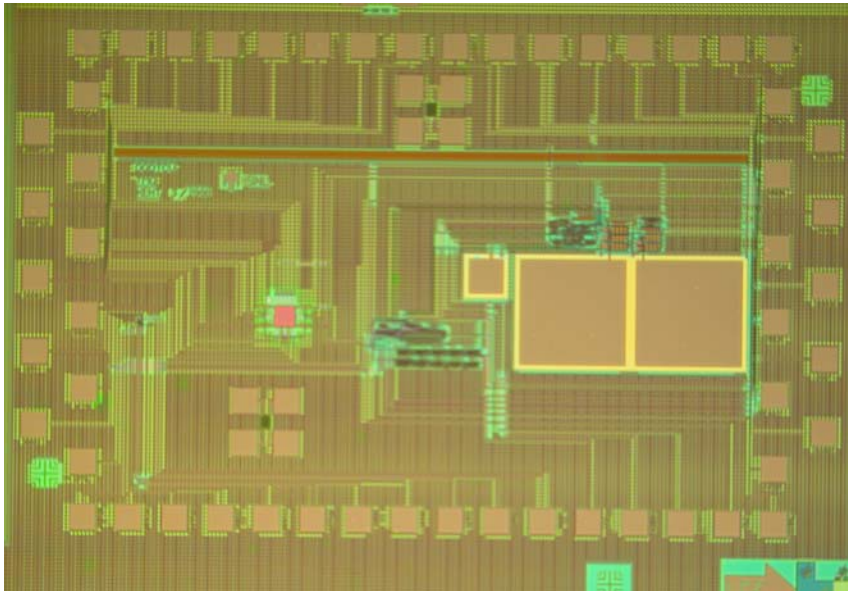


- Silicon on insulator *(SOI)*
- 7nm gate oxide
- 0.35 μm minimum feature
- Operation range 3.3 V

Multi-Project Wafer Program

1st generation ASIC contains:

- Current amplifier
- Current Comparator
- MUX circuitry
- FET which allows potential on chip DQD integration



(3x2mm)

Why is cryo-CMOS non-trivial?

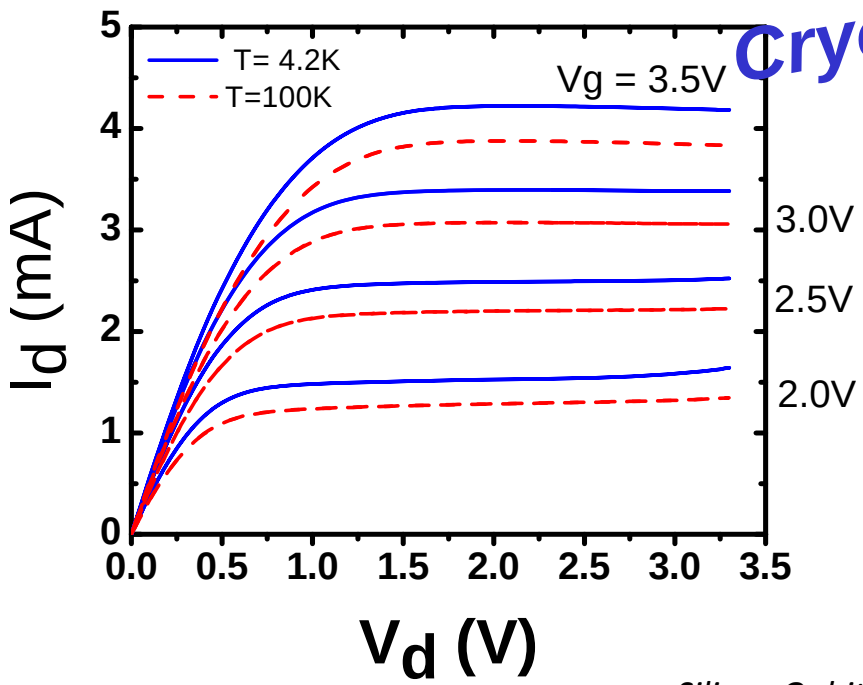
Effects of Low temp operation:

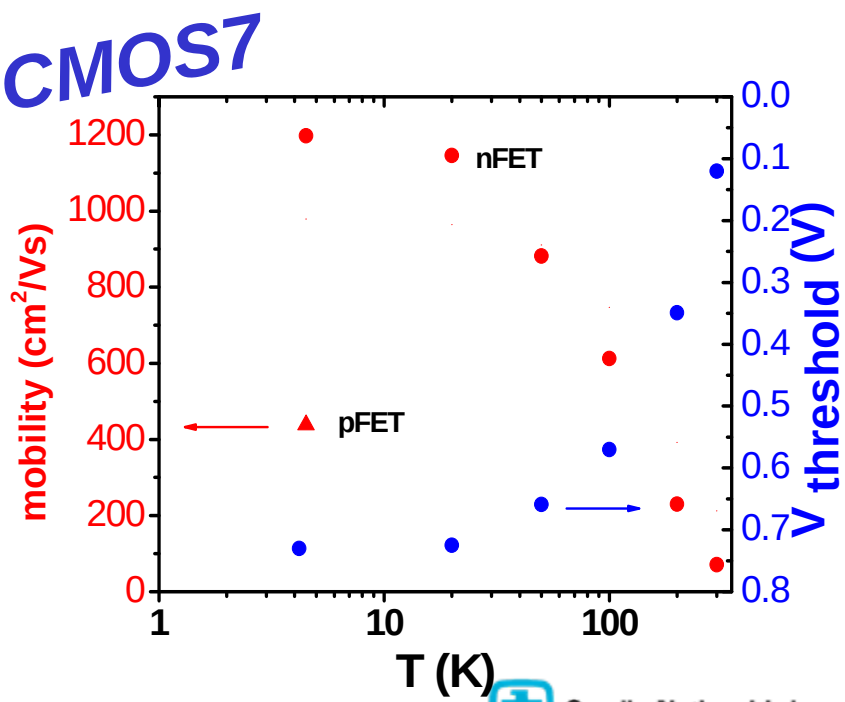
- Fermi level shift (freezeout of dopants)

  increase in threshold voltage, substrate resistance

- Reduction in electron-phonon scattering

  increase in carrier mobility, higher electron energies (impact ionization)

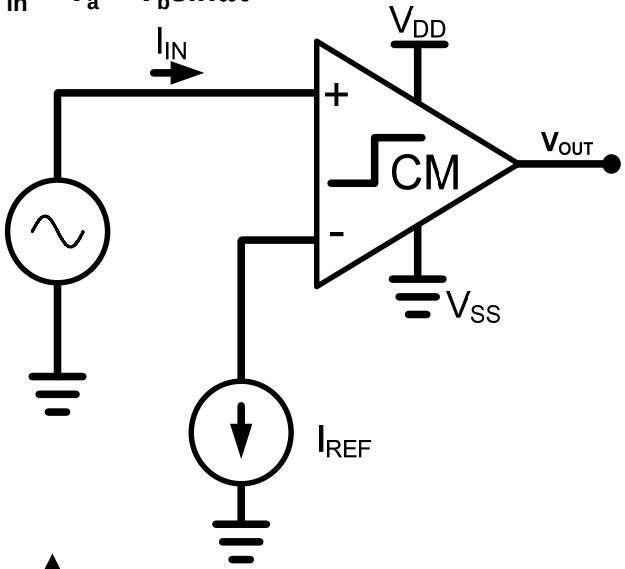


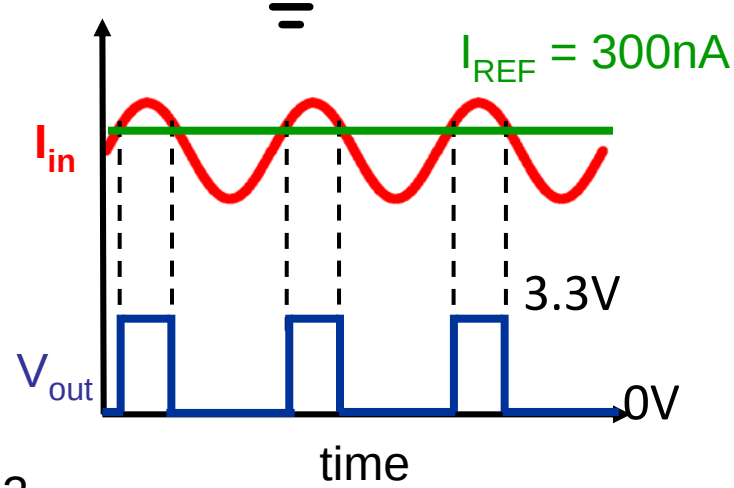


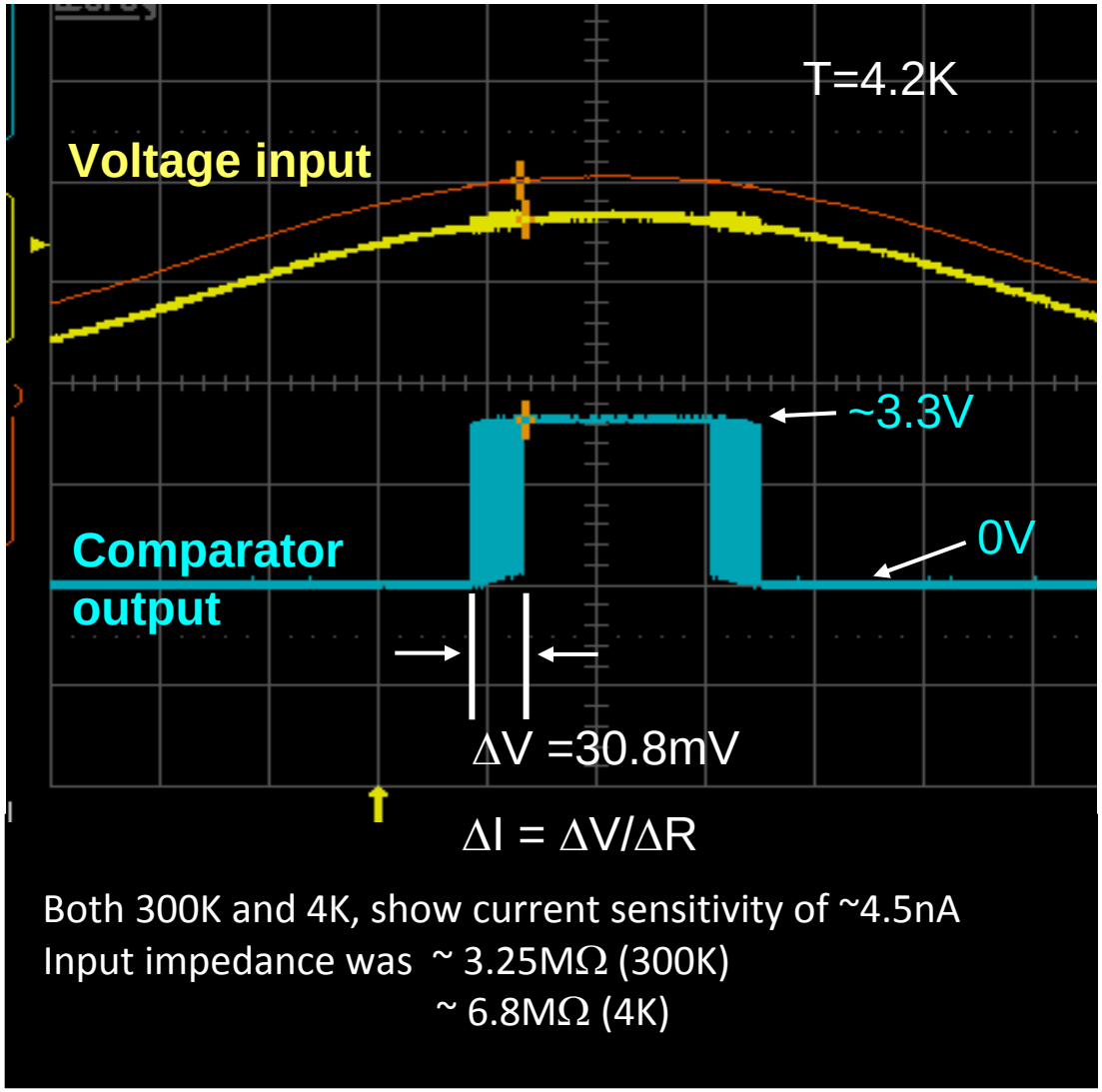
Current Comparator

Sensitivity Measurements

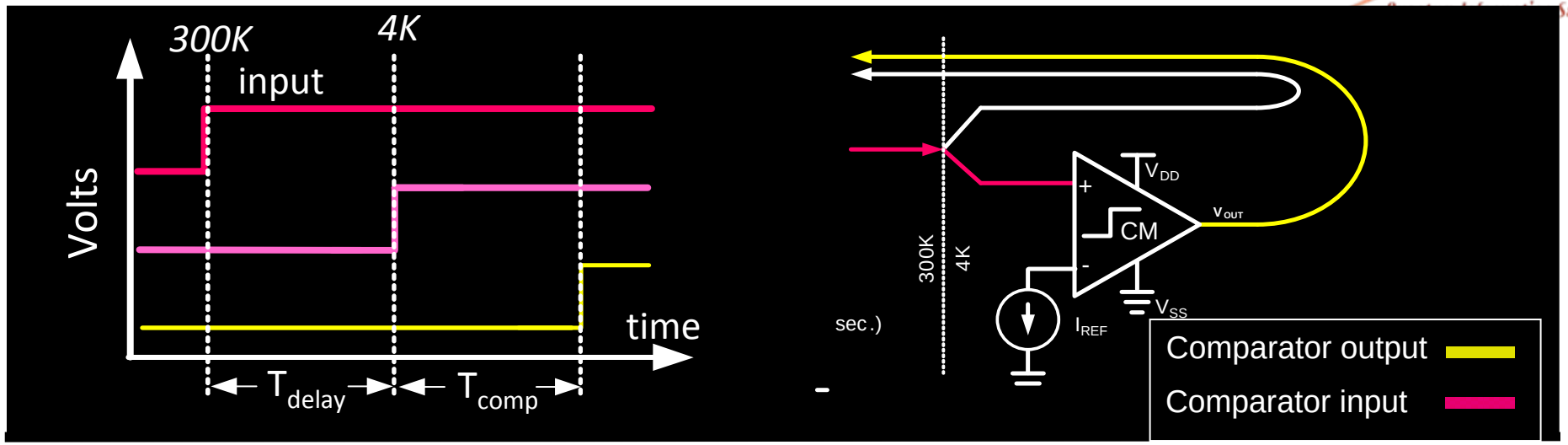
$V_{in} = V_a + V_b \sin\omega t$

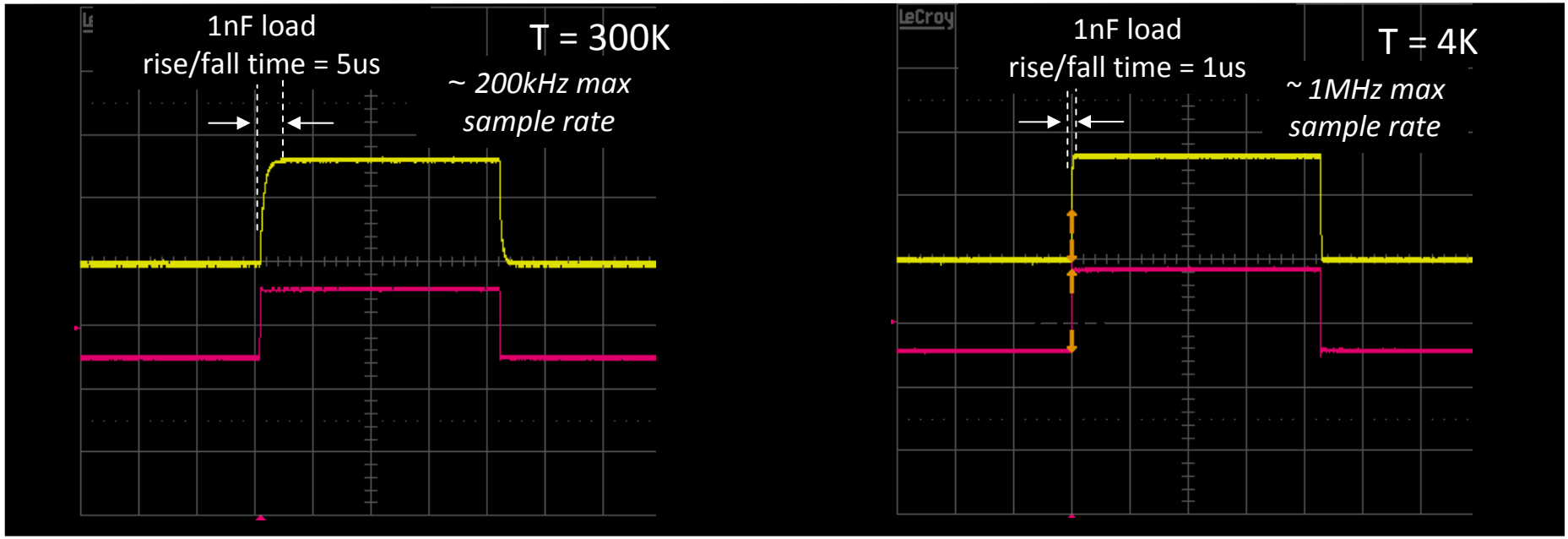




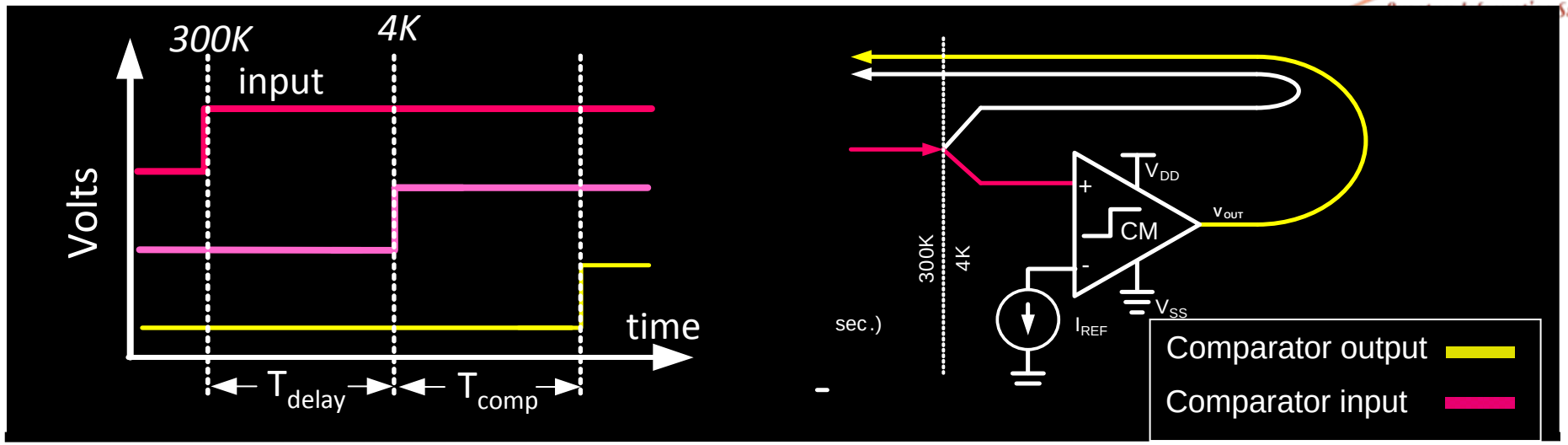


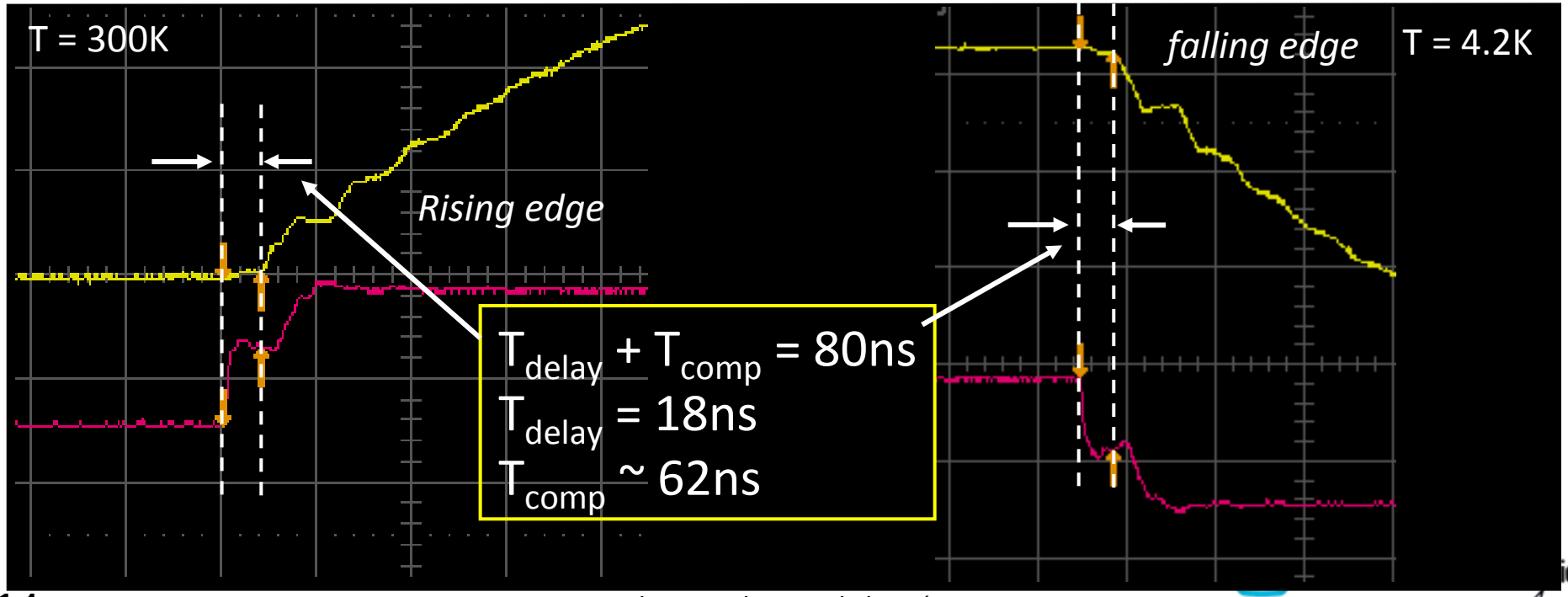
Comparator Speed





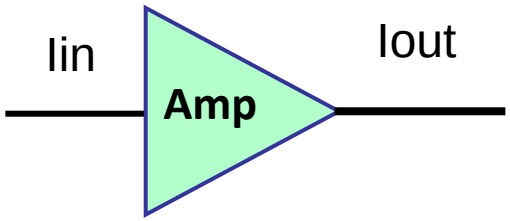
Comparator Speed

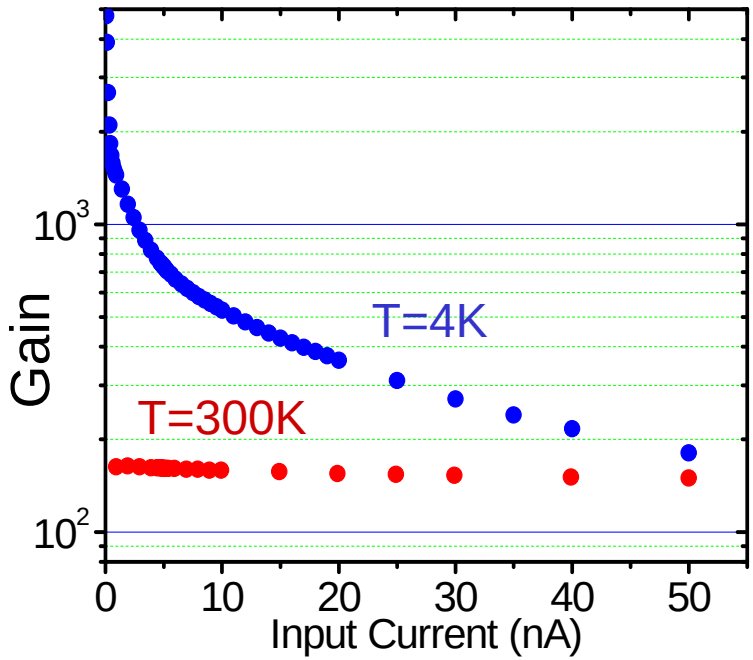




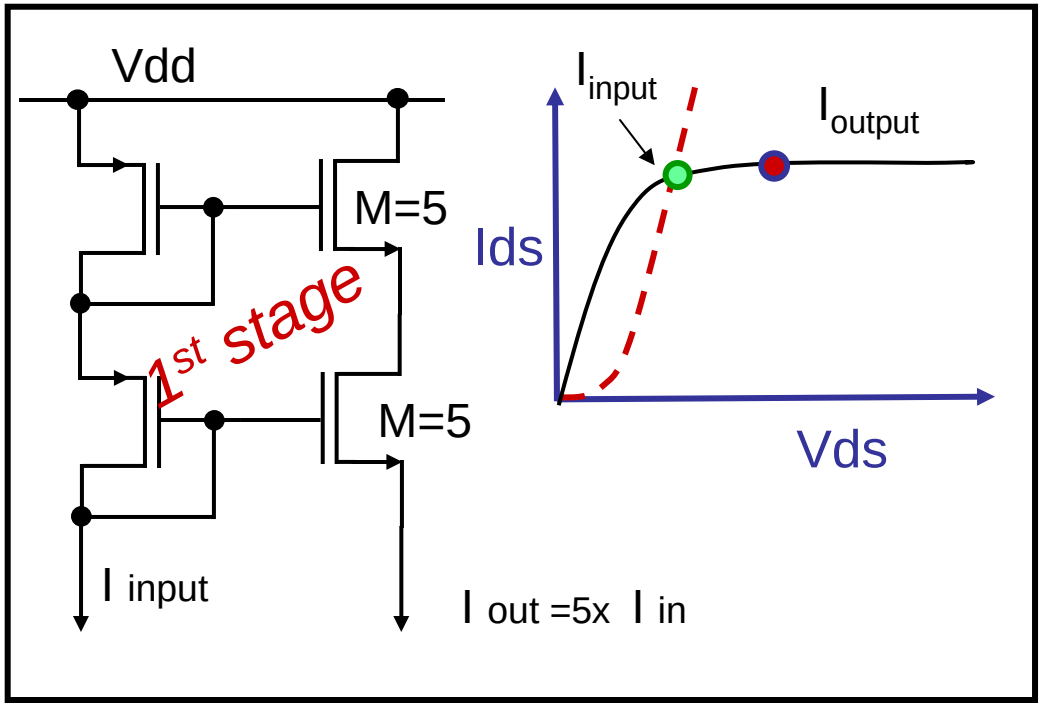
Current amplifier

Increase sensitivity of comparator with current to current amplifier

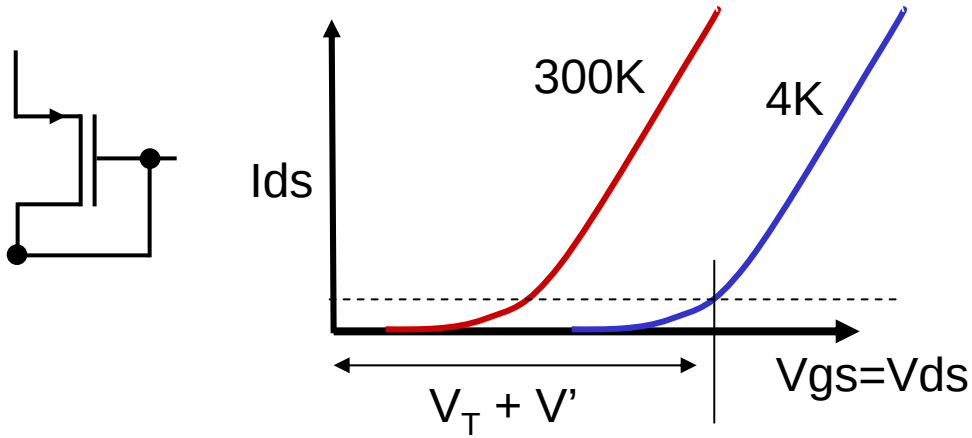


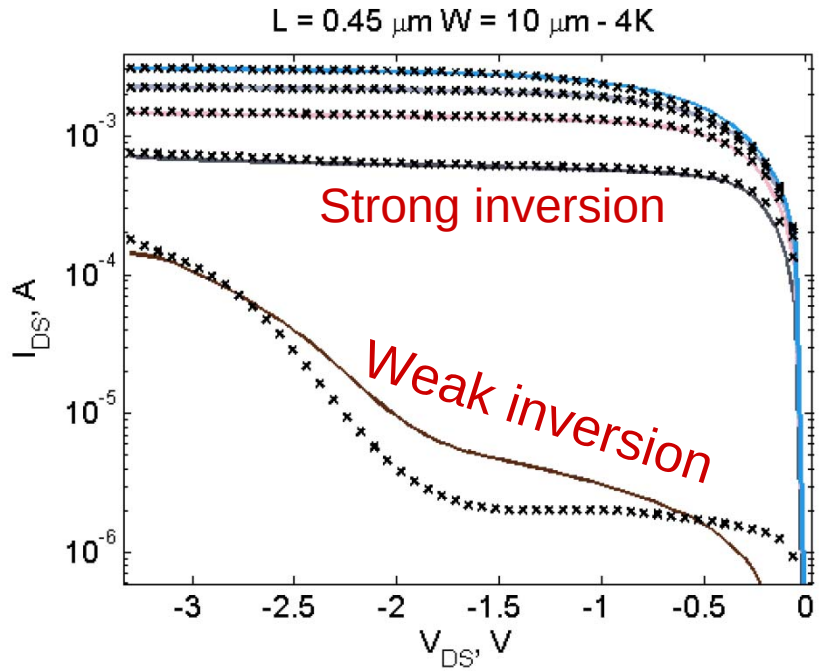


Cascode current mirror
(3 stages gain ~ 125)

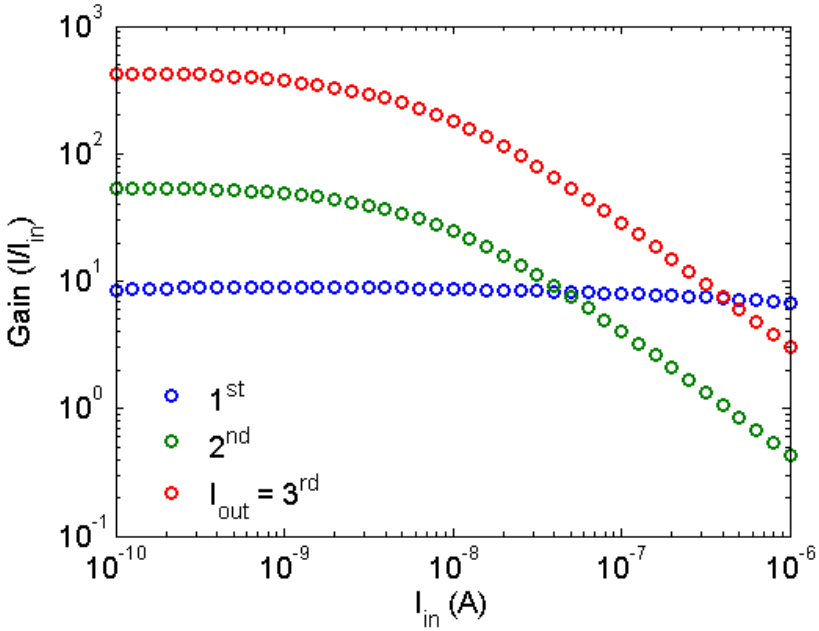


Cryo-Spice Modeling





Simulation of Current Amp



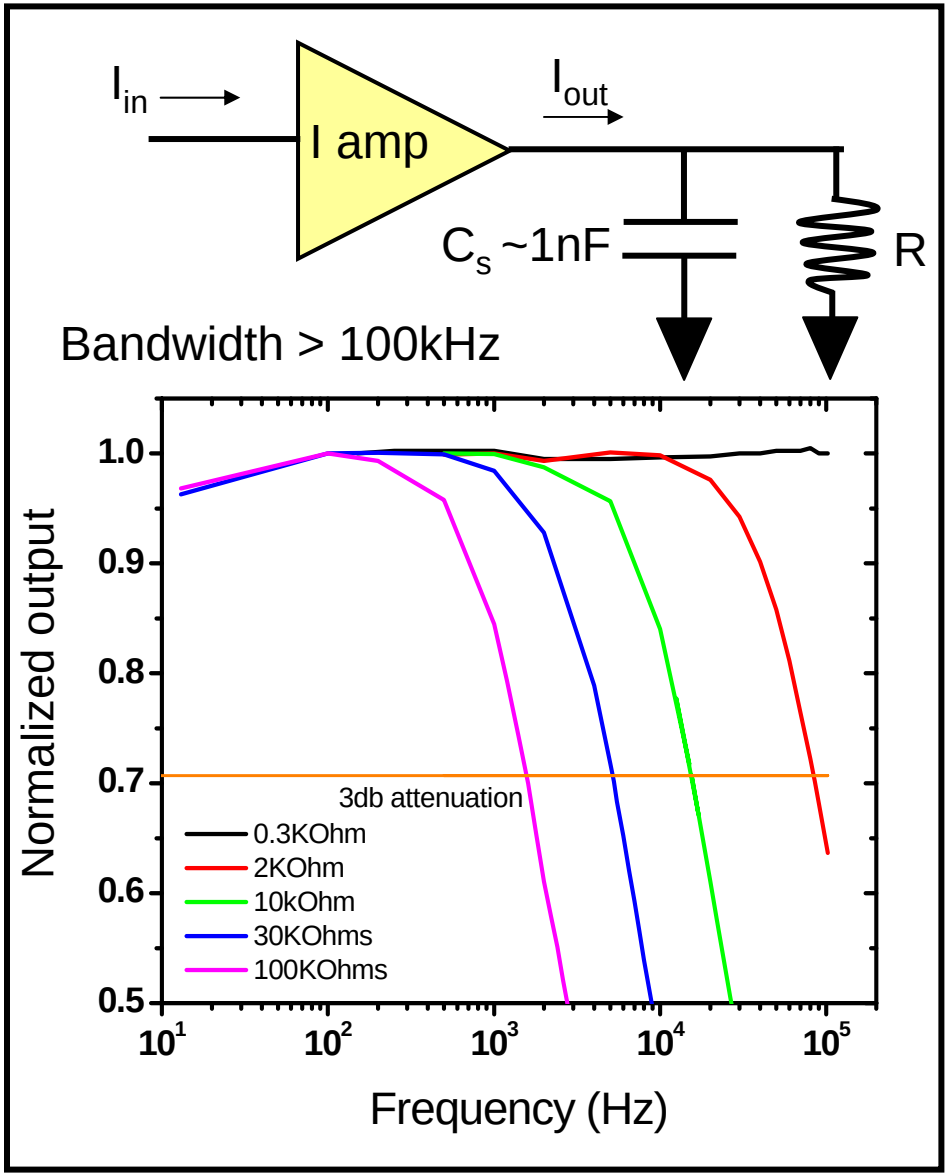
The increase in V_T:

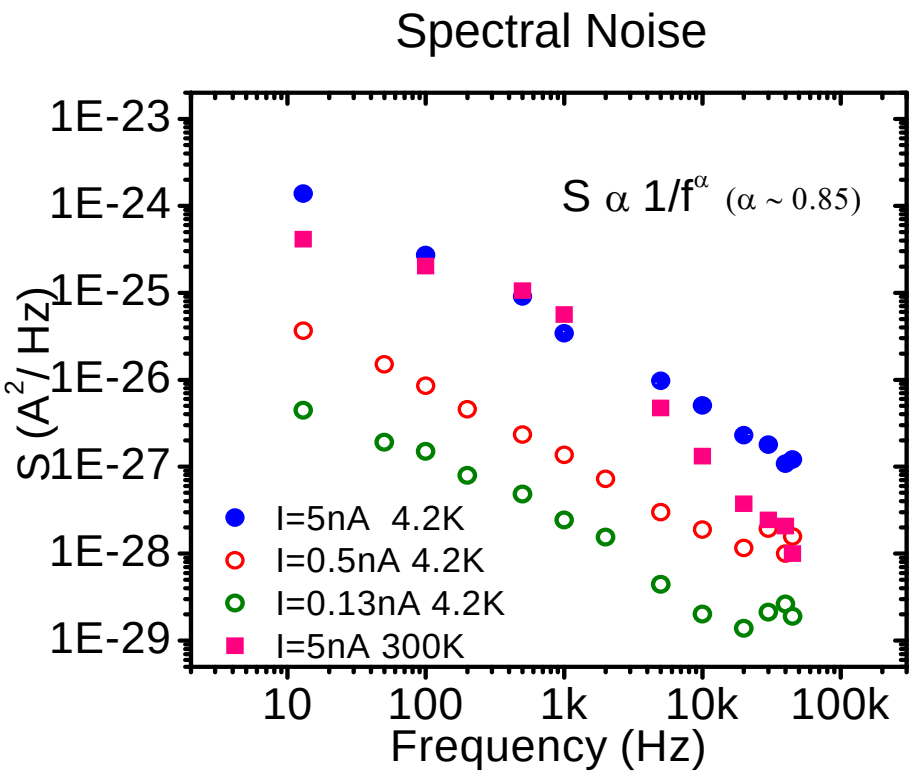
- operation in weak inversion
- matching becomes poor
- decrease in dynamic range

Next speaker:

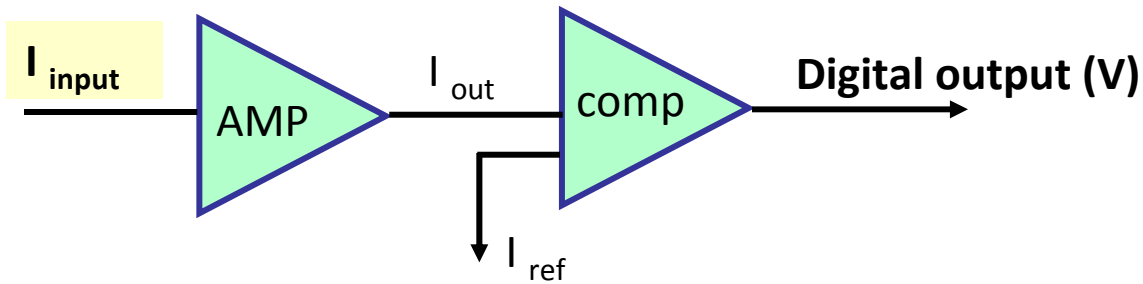
A. Akturk, " Compact modeling of cryo-CMOS circuits using Verilog-A"

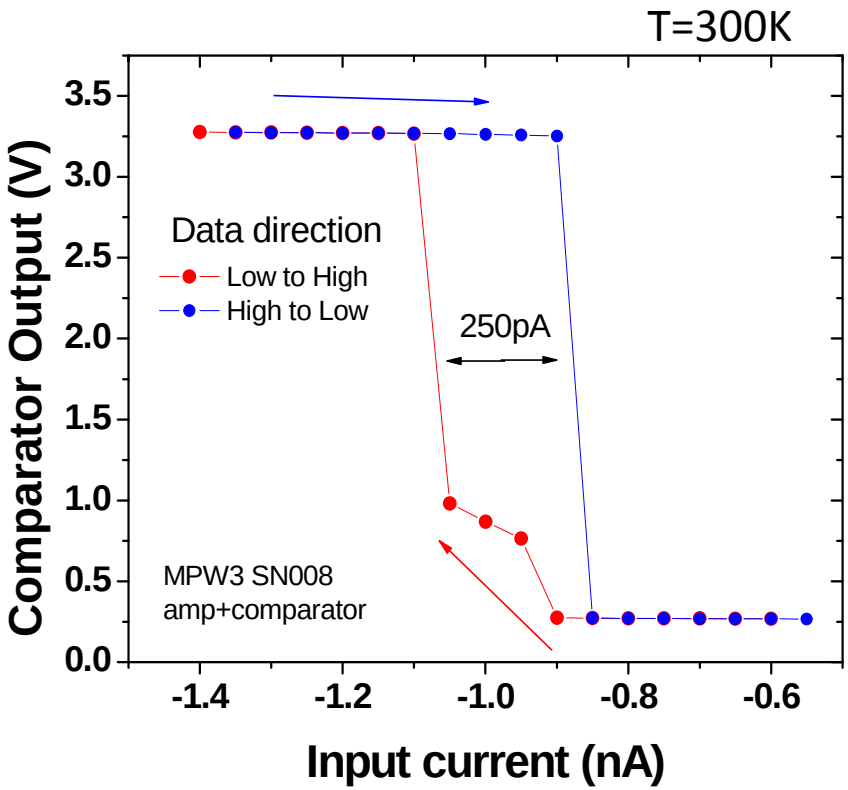
Amplifier Specs

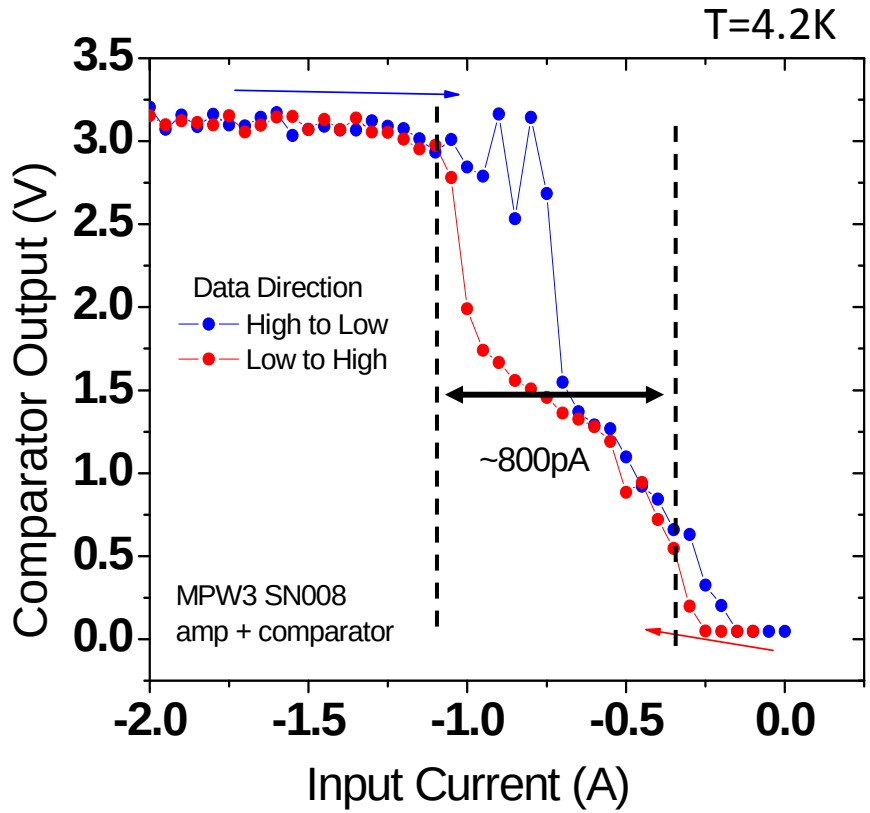




Sensitivity: Amp & Comparator







Where do we stand?

GaAs

APPLIED PHYSICS LETTERS **91**, 162101 (2007)

Fast single-charge sensing with a rf quantum point contact

D. J. Reilly and C. M. Marcus[a)]
Department of Physics, Harvard University, Cambridge, Massachusetts 02138, USA

M. P. Hanson and A. C. Gossard
Department of Materials, University of California, Santa Barbara, California 93106, USA

(Received 21 July 2007; accepted 28 August 2007; published online 15 October 2007)

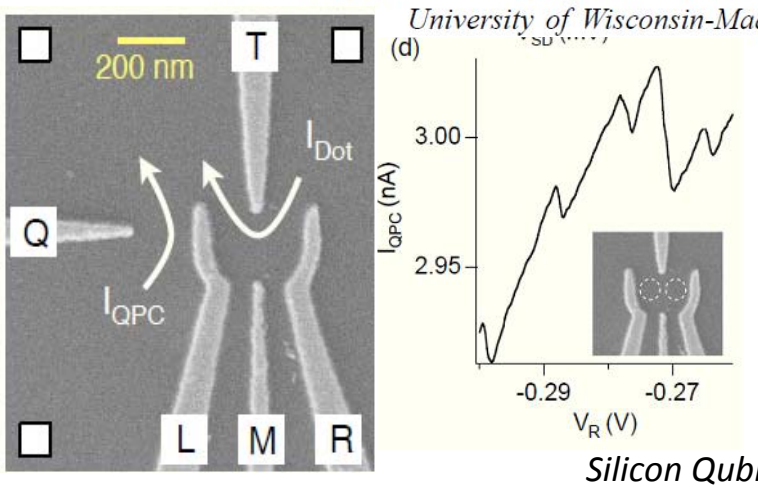
$\delta I \sim 100pA$

Si/SiGe

Charge sensing and controllable tunnel coupling in a Si/SiGe double quantum dot

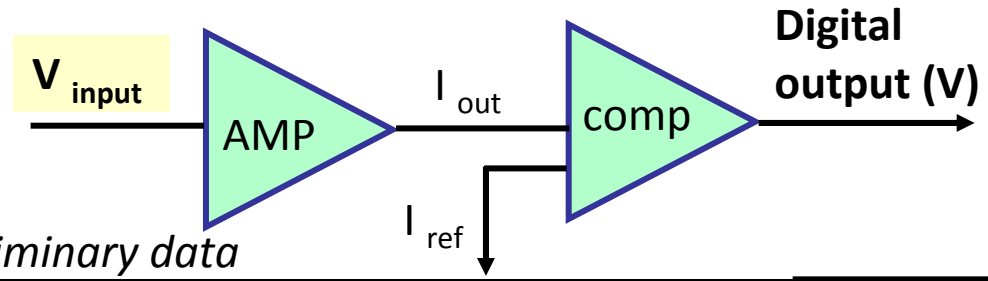
C. B. Simmons, Madhu Thalakulam, B. M. Rosemeyer, B. J. Van Bael, E. K. Sackmann,
D. E. Savage, M. G. Lagally, R. Joynt, M. Friesen, S. N. Coppersmith, and M. A. Eriksson
University of Wisconsin-Madison, Madison, Wisconsin 53706, USA

arXiv:0905.1647v1

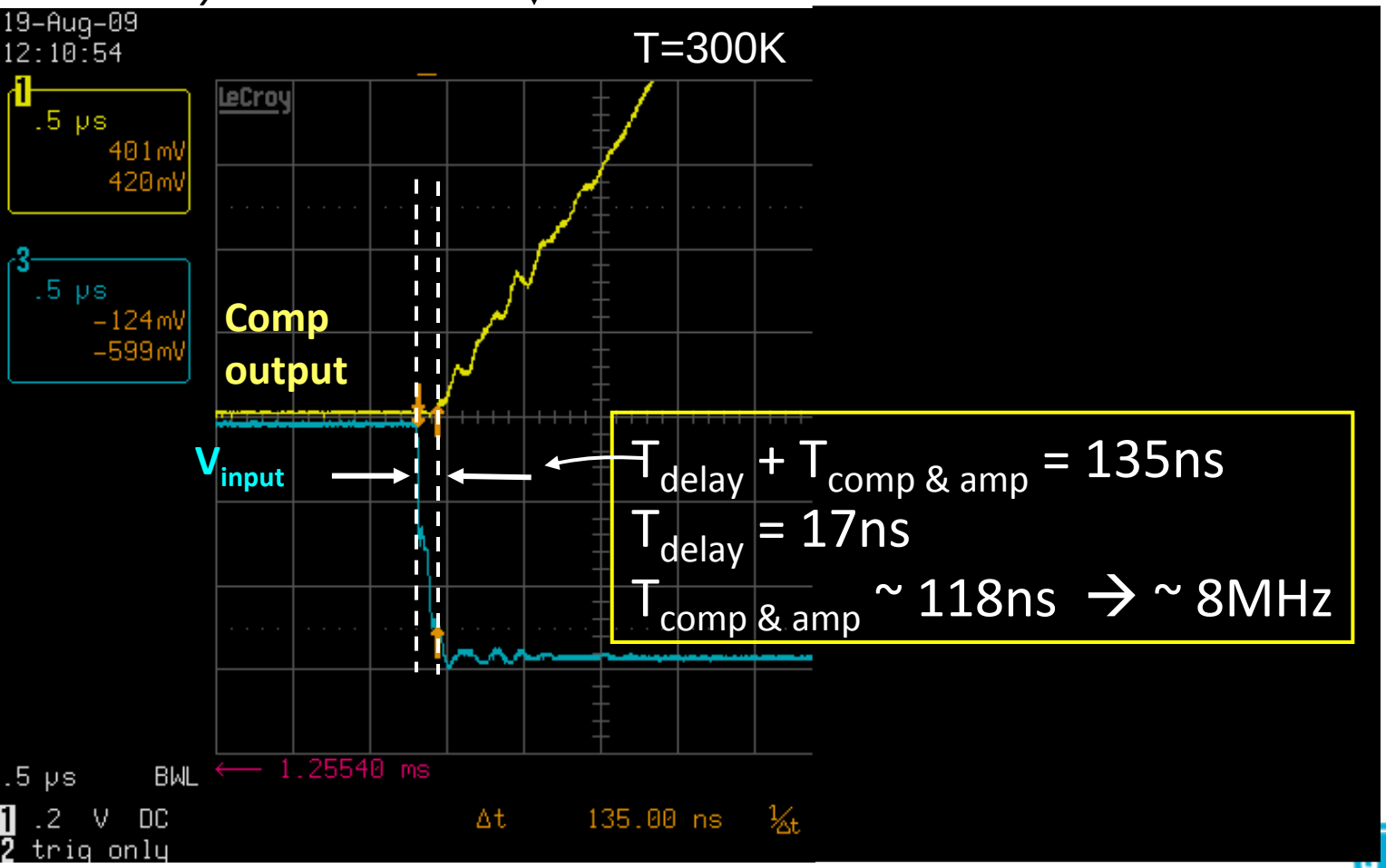


$\delta I = 50pA$

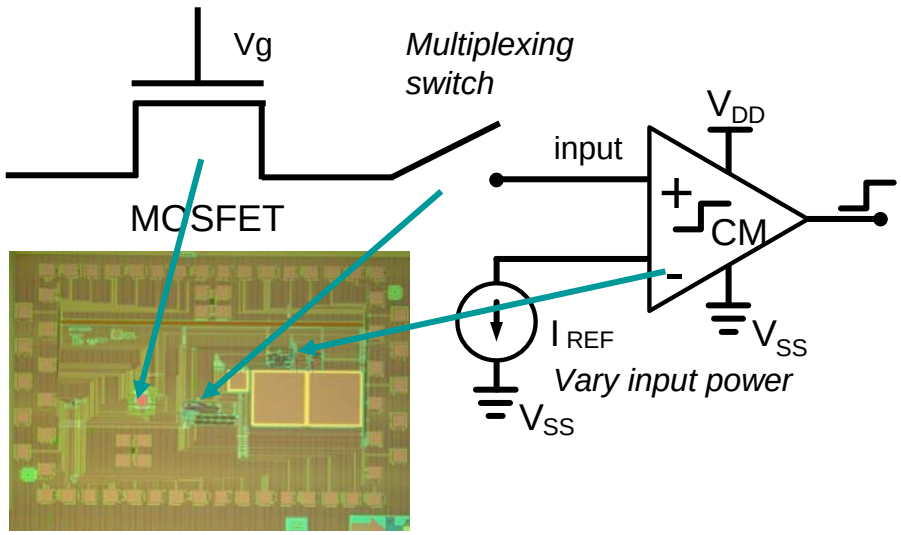
Speed of Amp & Comparator



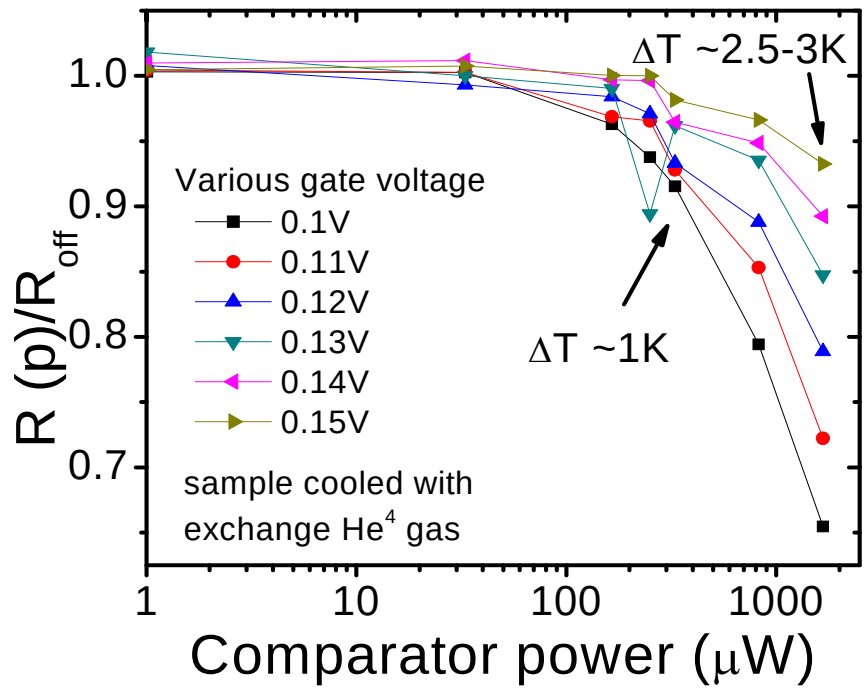
Preliminary data



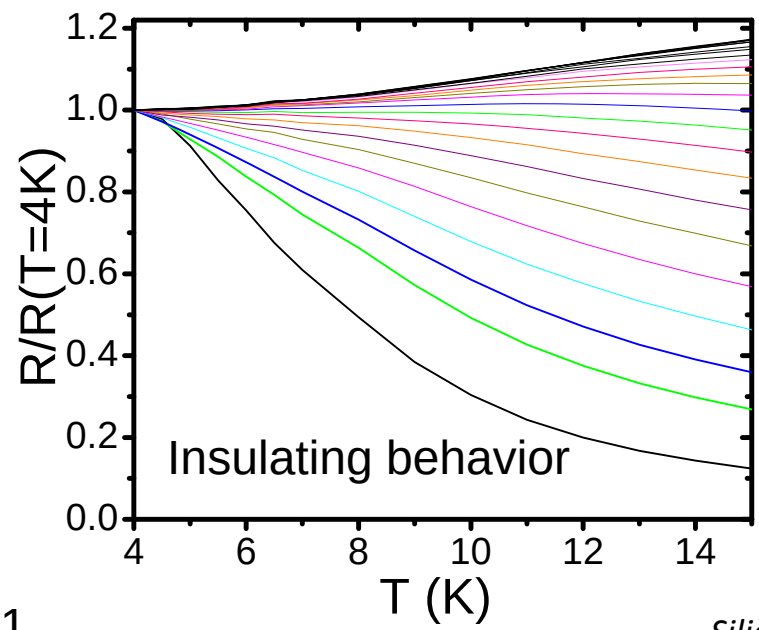
Heating due to Comparator



2. Measure changes in MOSFET resistance vs. comparator power



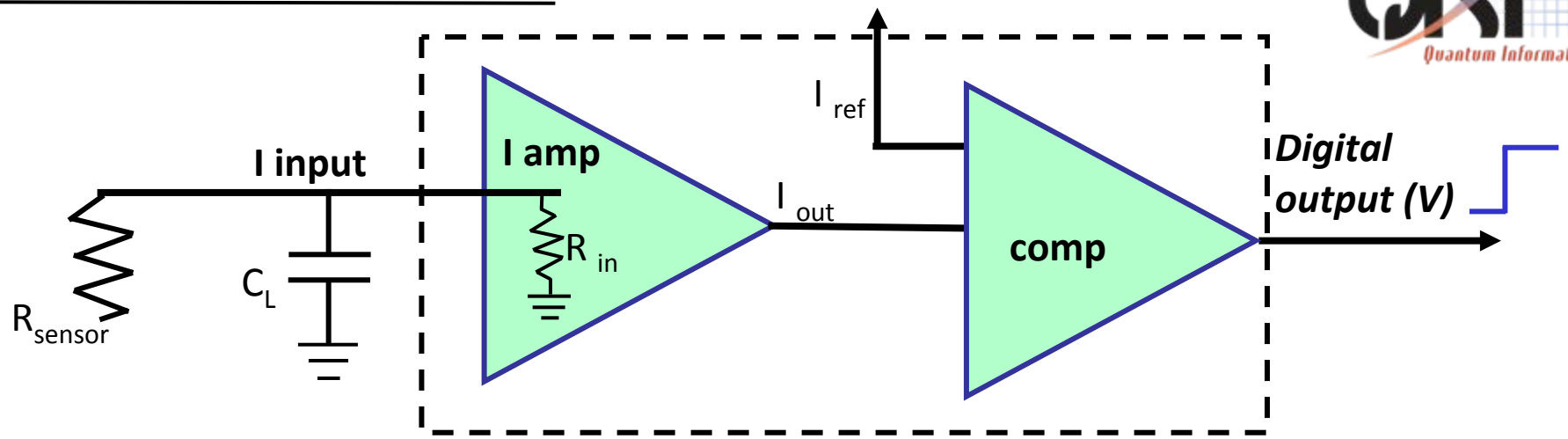
1. Use MOSFET as thermometer



Vg~0.1V

- Current amp will dissapate ~ μW

Assessment:



- Combined digital readout speed ~ 120ns with a 1-2μs rise fall time at 4K
- Power consumption is ~ 10μW, within cooling power of 4K, 1.5K pot and still
- Sensitivity of ΔI of the amp & comparator is within a factor ~4
- Input impedance of the amp will be a speed bump

Future Work: Solutions

Sensitivity:

- Improvements can be made by improving gain in amplifier

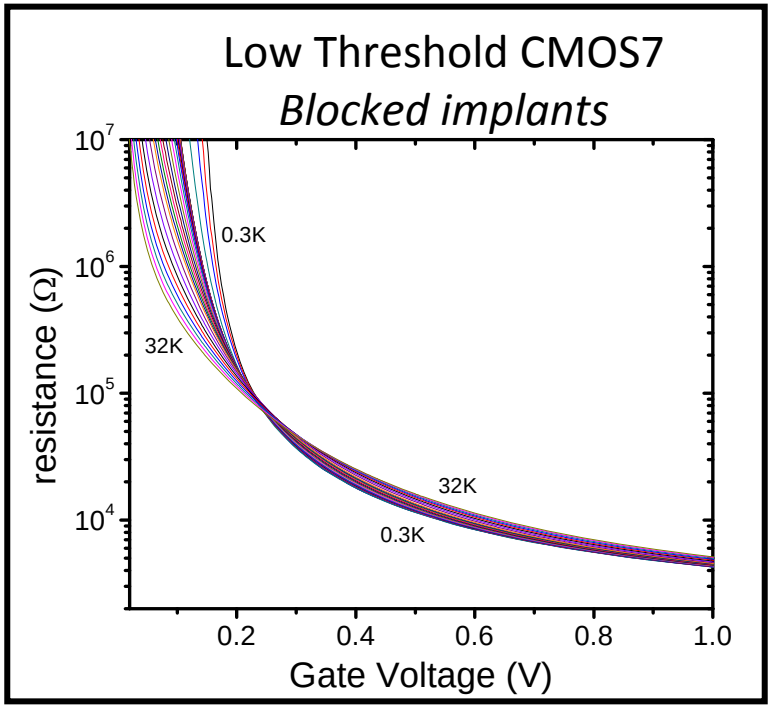
Speed:

- Rise/fall time can be mitigated by:
  - Larger driver
  - Data buffer at 4K
- Input impedance of the amp can be reduced via voltage regulator

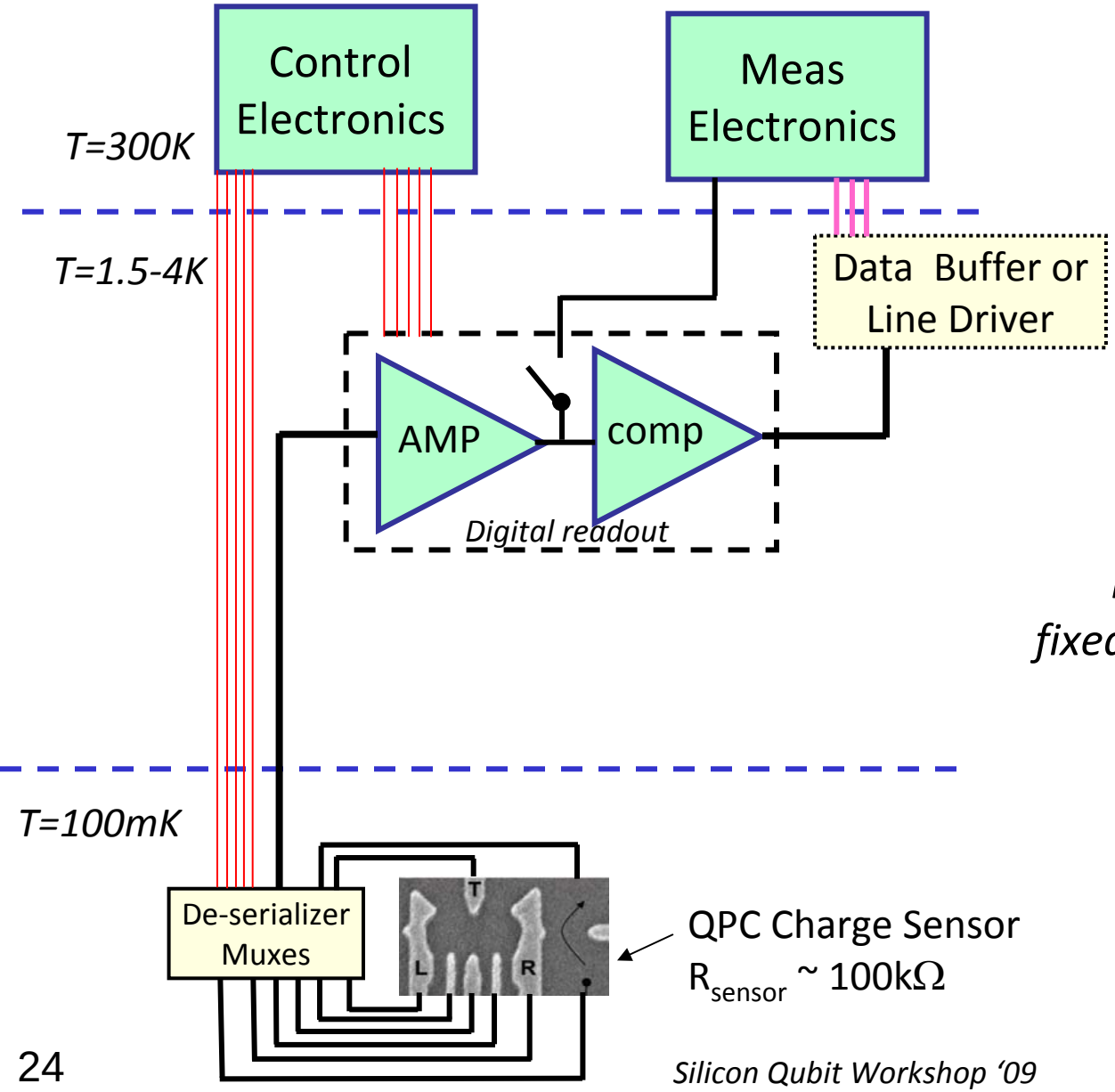
Investigating low threshold devices (alter CMOS7):

- Provide more dynamic range in operation
- Reduce input impedance

More modeling.



Implementation



Readout scheme not fixed to one material system

Summary

- Fabricated & Characterized cryo-CMOS circuits fabricated using Sandia's CMOS7 foundry process

- **Current Comparator**
  - can operate ~62ns
  - max sensitivity ~4.5nA

- **Current Amp:**
  - Bandwidth > 100kHz
  - Gain of 125 at 300K
    - 300-2000 at 4.2K
  - Input noise ~1pA/Hz1/2 at 10Hz

- **Comparator w amp**
  - Max ΔI sensitivity of 250pA
  - Speed of ~ 120ns
  - Power consumption ~ 10μW

- On chip MUX circuitry works at 4K

- Characterized CMO7 FETs and began developing SPICE modeling

NEXT TALK